VLSI AND EMBEDDED SYSTEM

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Lecturer (Electronics)

SYLLABUS

Th.2 VLSI & EMBEDDED SYSTEM

Theory	: 4 Periods per week	I.A.	: 20 Marks
Total Periods	: 60 Periods	Term End Exam	: 80 Marks
Examination	: 3 Hours	TOTAL MARKS	: 100 Marks

Chapter wise Distribution of periods with Total periods

Sl.No.	Topics	Periods
1.	Introduction to VLSI & MOS Transistor	12
2.	Fabrication of MOSFET	10
3.	MOS Inverter	09
4.	Static Combinational, Sequential, Dynamics logic circuits& Memories	15
5.	System Design method & Synthesis	04
6.	Introduction to Embedded Systems	10
	TOTAL	60

Detailed Contents:

Unit-1: Introduction to VLSI & MOS Transistor

1.1 Historical perspective- Introduction
1.2 Classification of CMOS digital circuit types
1.3 Introduction to MOS Transistor& Basic operation of MOSFET.
1.4 Structure and operation of MOSFET (n-MOS enhancement type) & COMS
1.5 MOSFET V-I characteristics,
1.6 Working of MOSFET capacitances.
1.7 Modelling of MOS Transistors including Basic concept the SPICE level-1 models, the level-2 and level-3 model.
1.8 Flow Circuit design procedures
1.9 VLSI Design Flow & Y chart
1.10 Design Hierarchy
1.11 VLSI design styles-FPGA, Gate Array Design, Standard cells based, Full custom

Unit-2: Fabrication of MOSFET

2.1 Simplified process sequence for fabrication
2.2 Basic steps in Fabrication processes Flow
2.3 Fabrication process of nMOS Transistor
2.4 CMOS n-well Fabrication Process Flow
2.5 MOS Fabrication process by n-well on p-substrate
2.6 CMOS Fabrication process by P-well on n-substrate
2.7 Layout Design rules
2.8 Stick Diagrams of CMOS inverter

Unit-3: MOS Inverter

3.1 Basic nMOS inverters,
3.2 Working of Resistive-load Inverter
3.3 Inverter with n-Type MOSFET Load – Enhancement Load, Depletion n-MOS inverter
3.4 CMOS inverter – circuit operation and characteristics and interconnect effects: Delay time definitions
3.5 CMOS Inventor design with delay constraints – Two sample mask lay out for p-type substrate.

Unit-4: Static Combinational, Sequential, Dynamics logic circuits & Memories

4.1 Define Static Combinational logic ,working of Static CMOS logic circuits (Two-input NAND Gate)
4.2 CMOS logic circuits (NAND2 Gate)
4.3 CMOS Transmission Gates(Pass gate)
4.4 Complex Logic Circuits - Basics
4.5 Classification of Logic circuits based on their temporal behaviour
4.6 SR Flip latch Circuit,
4.7 Clocked SR latch only.
4.8 CMOS D latch.
4.9 Basic principles of Dynamic Pass Transistor Circuits
4.10 Dynamic RAM, SRAM,
4.11 Flash memory

Unit-5: System Design method & synthesis

5.1 Design Language (SPL & HDL)& HDL & EDA tools & VHDL and packages Xilinx
5.2 Design strategies & concept of FPGA with standard cell based design
5.3 VHDL for design synthesis using CPLD or FPGA
5.4 Raspberry Pi - Basic idea

Unit-6: Introduction to Embedded Systems

6.1 Embedded Systems Overview,list of embedded systems,characteristics ,example – A Digital Camera

6.2 Embedded Systems Technologies--Technology – Definition
-Technology for Embedded Systems
-Processor Technology
-IC Technology

6.3 Design Technology-Processor Technology,General Purpose Processors – Software, Basic Architecture of Single Purpose Processors – Hardware

6.4 Application – Specific Processors,Microcontrollers,Digital Signal Processors(DSP)

6.5 IC Technology- Full Custom / VLSI,Semi-Custom ASIC (Gate Array & Standard Cell), PLD (Programmable Logic Device)

6.6 Basic idea of Arduino micro controller

Coverage of Syllabus upto Internal Exams

Chapter 1,2,3,4

Books Recommended:

1. COMS Digital integrated Circuits –Analysis & Design –Sung Mo-Kang &YussufLeblebici, TMH.
2. VLSI Design AND EDA Tools by A. Sarkar,S.De,Chandran Kumar Sarkar –SCITECH (Reference)
3. Embedded System Design –Frank Vahid& Tony Givargis-WILEY India.
4. VLSI Design by Sakthiver. R – S chand. (Reference)
5. VHDL Programing by Example by Douglas L. Perry-TMH

LESSON PLAN

Th2. VLSI AND EMBEDDED SYSTEM -5TH SEMESTER ETC		
Week	**No of Periods Allotted (60)**	**Syllabus To be Covered**
1ST	**1. Introduction to VLSI & MOS Transistor**	
	1.1	Historical perspective- Introduction
	1.2	Classification of CMOS digital circuit types
	1.3	Introduction to MOS Transistor& Basic operation of MOSFET.
	1.4	Structure and operation of MOSFET (n-MOS enhancement type) & CMOS
2ND	**1.5**	MOSFET V-I characteristics.
	1.6	Working of MOSFET capacitances.
	1.7	Modelling of MOS Transistors including Basic concept the SPICE level-1 models, the level-2 and level-3 model.
	1.8	Flow Circuit design procedures
3RD	**1.9**	VLSI Design Flow & Y chart
	1.10	Design Hierarchy

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	2.1	Simplified process sequence for fabrication
	2.2	Basic steps in Fabrication processes Flow
	2.3	Fabrication process of nMOS Transistor
	2.4	CMOS n-well Fabrication Process Flow
5TH	**2.5**	MOS Fabrication process by n-well on p-substrate
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	2.6	CMOS Fabrication process by P-well on n-substrate
	2.6	CMOS Fabrication process by P-well on n-substrate
6TH	**2.7**	Layout Design rules
	2.8	Stick Diagrams of CMOS inverter
	3. **MOS Inverter**	
	3.1	Basic nMOS inverters
	3.2	Working of Resistive-load Inverter
7TH	**3.2**	Working of Resistive-load Inverter
	3.3	Inverter with n-Type MOSFET Load – Enhancement Load, Depletion n-MOS inverter
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	4. **Static Combinational, Sequential, Dynamics logic circuits & Memories**	
	4.1	Define Static Combinational logic, working of Static CMOS logic circuits (Two-input NAND Gate)
9TH	**4.2**	CMOS logic circuits (NAND2) Gate
	4.3	CMOS Transmission Gates (Pass gate)
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	4.6	SR Flip latch Circuit
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	4.7	Clocked SR latch only.
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	4.8	CMOS D latch.
	4.9	Basic principles of Dynamic Pass Transistor Circuits
	4.10	Dynamic RAM, SRAM
12TH	**4.10**	Dynamic RAM, SRAM
	4.11	Flash memory
	5. **System Design method & synthesis**	
	5.1	Design Language (SPL & HDL) & HDL & EDA tools & VHDL and packages Xilinx
	5.2	Design strategies & concept of FPGA with standard cell-based design

	5.3	VHDL for design synthesis using CPLD or FPGA
	5.4	Raspberry Pi - Basic idea
	6. **Introduction to Embedded Systems**	
	6.1	Embedded Systems Overview, list of embedded systems, characteristics, example – A Digital Camera
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14TH	**6.2**	Embedded Systems Technologies--Technology – Definition -Technology for Embedded Systems -Processor Technology -IC Technology
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	6.3	Design Technology-Processor Technology, General Purpose Processors – Software, Basic Architecture of Single Purpose Processors – Hardware
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15TH	**6.4**	Application – Specific Processors, Microcontrollers, Digital Signal processors (DSP)
	6.5	IC Technology- Full Custom / VLSI, Semi-Custom ASIC (Gate Array & Standard Cell), PLD (Programmable Logic Device)
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	6.6	Basic idea of Arduino micro controller

PO Statements:

PO1	**Basic and Discipline specific knowledge**	Apply knowledge of basic mathematics, science and engineering fundamentals and engineering specialization to solve the engineering problems.
PO2	**Problem analysis**	Identify and analyze well-defined engineering problems using codified standard methods
PO3	**Design/development of solutions**	Design solutions for well-defined technical problems and assist with the design of systems components or processes to meet specified needs.
PO4	**Engineering Tools, Experimentation and Testing**	Apply modern engineering tools and appropriate technique to conduct standard tests and measurements
PO5	**Engineering practices for society, sustainability and environment**	Apply appropriate technology in context of society, sustainability, environment and ethical practices.
PO6	**Project Management**	Use engineering management principles individually, as a team member or a leader to manage projects and effectively communicate about well-defined engineering activities
PO7	**Life-long learning**	Ability to analyze individual needs and engage in updating in the context of technological changes

PSO Statements:

PSO1	Demonstrate technical competency in the design and analysis of electronics and telecommunication systems using various software and hardware tools
PSO2	Identify real time problems and provide energy and cost-efficient solutions using the knowledge of basic science, mathematics and Electronics and Telecommunication Engineering.

C303	**CO Statements**	CO related to POs
C303.1	Derive the current equation and plot the IV – characteristics of a MOS transistor.	PO1, PO2, PO3
C303.2	Draw the VLSI fabrication steps of nMOS, pMOS and CMOS. Categorise the hardware design in VLSI using Y chart.	PO1, PO3, PO4, PSO1
C303.3	Construct the VTC of CMOS inverter. Design combinational and sequential CMOS logic circuits.	PO1, PO2, PO3, PO4, PSO1, PSO2
C303.4	Develop VHDL code for combinational circuits.	PO4, PO7, PSO1, PSO2

CO – PO/PSO Matrix

C303	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**
C303.1	2	3	3						
C303.2	1		3	2				1	
C303.3	1	3	3	3				3	3
C303.4				2			3	3	3

Historical Perspective – Introduction

- BJT and Vacuum tube lost the battle in digital design due to
  - Large power consumption per unit area.
  - Upper limit on number of gates that can be integrated on a chip.
- MOS digital integrated circuits were looked at as alternatives.
- First MOS based IC – (PMOS only) used in calculators.
- 2nd age of digital ICs
  - First µP by INTEL (1972) – (NMOS only) (the 4004) [Faggin72]
  - In 1974 – (NMOS only) (the 8080) [Shima74]
- NMOS Logic is faster than PMOS; but failed in high density integration due to power issue.
- Finally, CMOS technology comes and this is where we still are today.
- **Moore's law**: Gordon Moore predicted that the number of transistors that ca be integrated on a single die would grow exponentially with time.

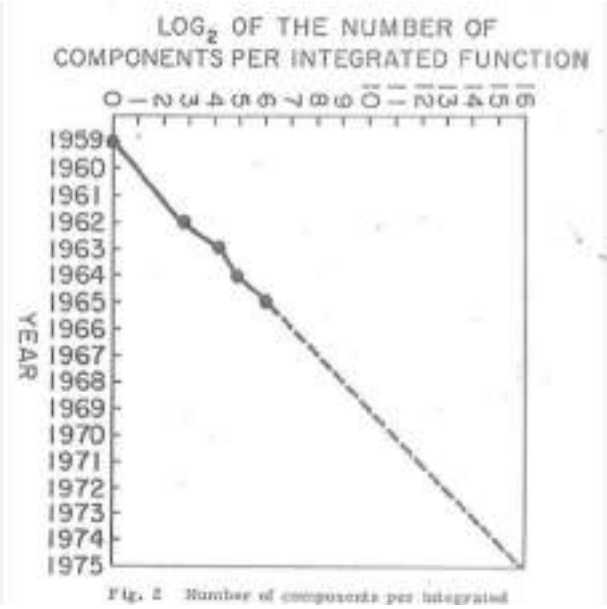
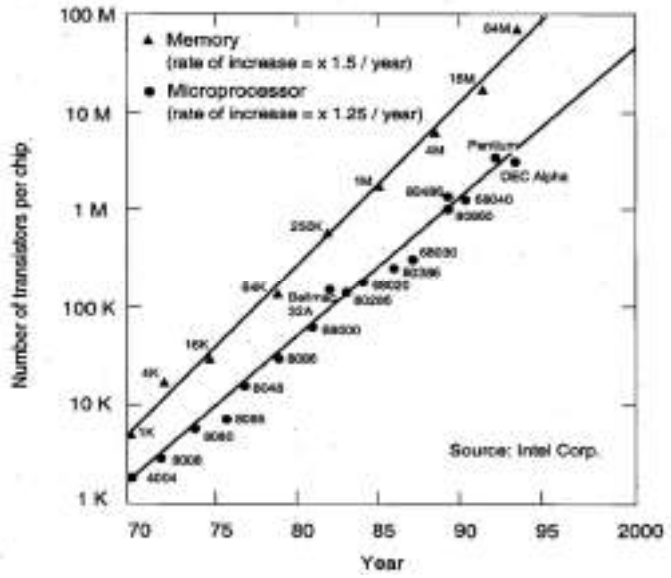


Fig. 2 Number of components per integrated

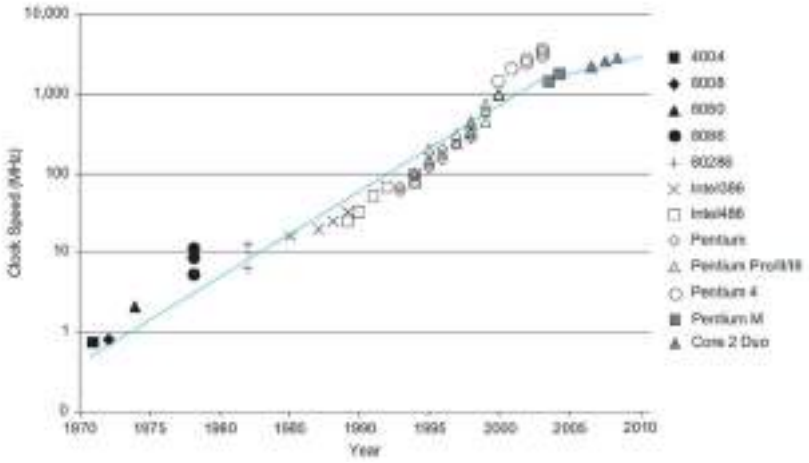
- Evolution of logic complexity in IC

ERA	DATE	COMPLEXITY (# of logic blocks per chip)
Single Transistor	1958	<1
Unit logic (One gate)	1960	1
Multi-function	1962	2 – 4
Complex function	1964	5 – 20
MSI	1967	20 – 200
LSI	1972	200 – 2000
VLSI	1978	2000 – 20000
ULSI	1989	>20000
	2021	billions

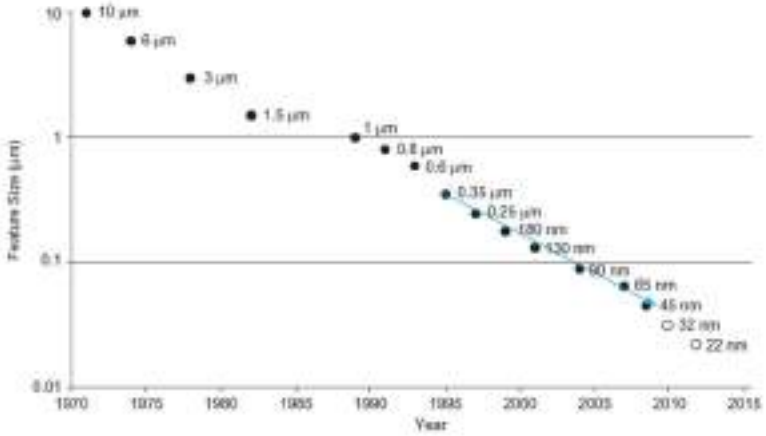
- Graph – (Number of transistors per chip)



- Graph – (Clock Speed)



- Graph – (Minimum feature Size)



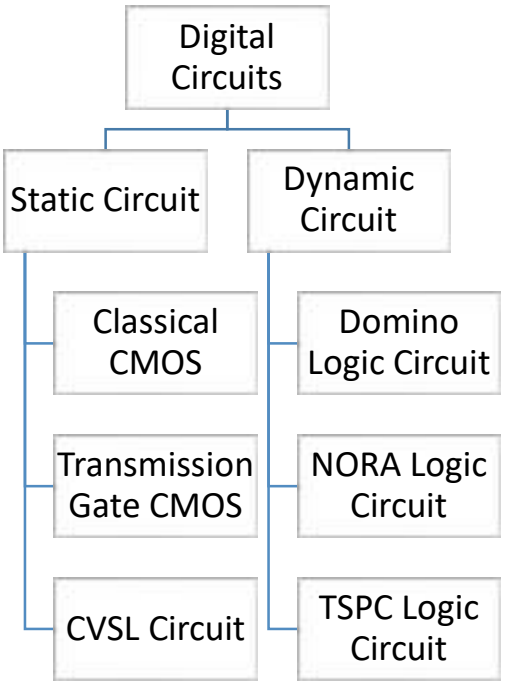
- Advantages of VLSI
    - Less area/volume and therefore, compactness
    - Less power consumption
    - Less testing requirements at system level
    - Higher reliability, mainly due to improved on-chip interconnects
    - Higher speed, due to significantly reduced interconnection length
    - Significant cost savings

Classification of CMOS Digital circuit type

Digital CMOS ICs are the driving force behind VLSI for high performance computing and other scientific and engineering applications. The Digital CMOS ICs have

- Low power
- Reliable performance
- Circuit techniques for high speed such as dynamic circuits

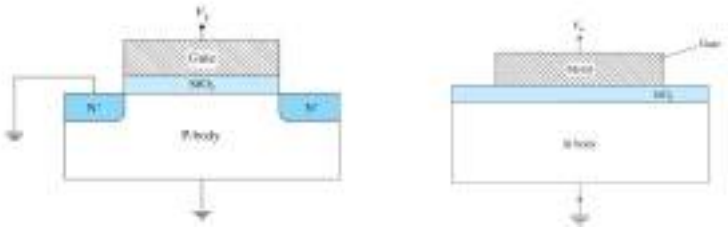
- Ongoing improvements in processing technology



CVSL – Cascaded Voltage Switch Logic
TSPC – True Single-Phase Clock

MOS Capacitor (Supplement Reading)

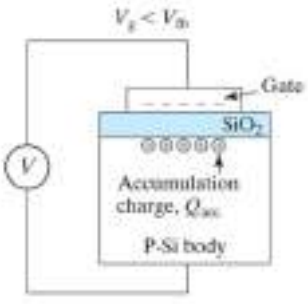
- MOSFET (MOS Transistor) is the fundamental building block of CMOS.
- A MOS transistor is a MOS Capacitor with 2 PN junctions flanking the capacitor.



- MOS

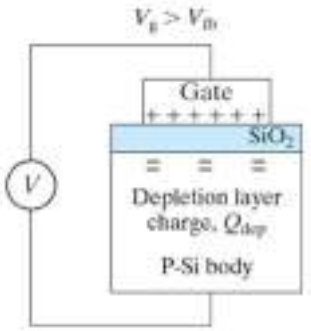
M	•Metal Gate •Al or Heavily doped Poly Si
O	•Oxide •SiO_2 as thin as 1.5nm (Dielectric)
S	•Semiconductor •Si body or substrate

- Operation of P-body MOS Capacitor
  a. Surface accumulation



  - V_{fb} : Flat band voltage (≈-0.7 V)
  - Holes accumulate near the surface when more negative Gate Voltage (V_g) than V_{fb} is applied.

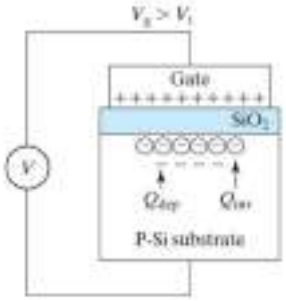
  b. Surface depletion



- When more positive V_g than V_{fb} is applied holes are depleted from the surface
- <u>Threshold of inversion</u>
  If we make V_g more and more positive, the surface is no longer in depletion; but at the threshold of inversion. The surface is inverted from P-type to N-type or electron rich. Threshold is defined as the condition when the surface electron concentration is equal to the bulk doping concentration.

$$\boldsymbol{V_t = 0.3\ to\ 1.0\ V}$$

c. Strong inversion beyond threshold

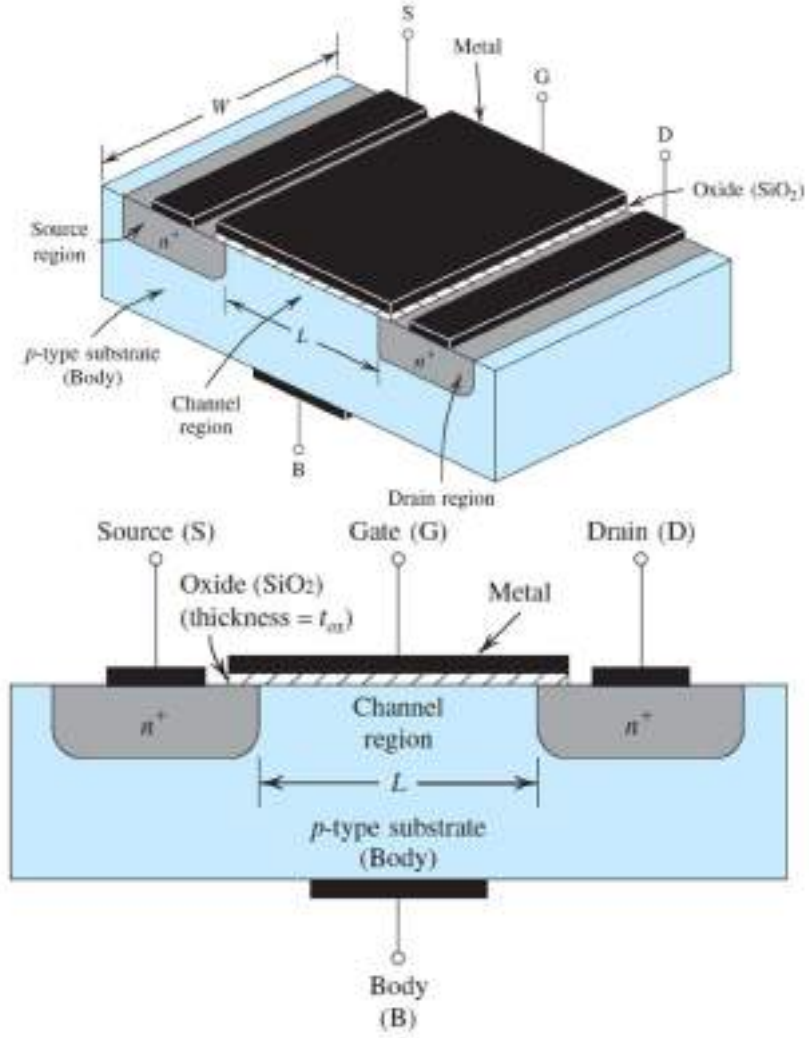


- When $V_g > V_t$, there is an inversion layer. MOS Capacitor in strong inversion behaves like a capacitor except for an offset voltage of V_t
- At $\boldsymbol{V_g = V_t}$, $\boldsymbol{Q_{inv} = 0}$

$$\boldsymbol{Q_{inv} = -C_{ox}(V_g - V_t)}$$

Structure and Operation of MOSFET

- **Construction**

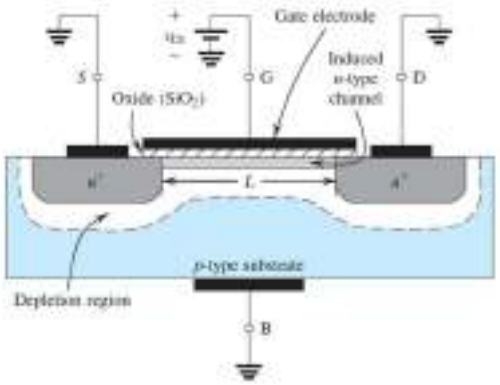


Body(B)	•Transistor is fabricated P - type substrate (body)
Source(S)	• heavily doped n-type (n+) created in the substrate.
Drain(D)	•heavily doped n-type (n+) created in the substrate
Gate(G)	•A thin SiO_2 layer grown on the surface of substrate. •Metal is deposited on top of oxide to form Gate electrode

- **Dimensions of MOSFET**
  - **L:** Length of channel (.03µm – 1µm)
  - **W:** Width of Channel (.05µm - 100µm)
  - $\boldsymbol{t_{ox}}$**:** Oxide thickness (1nm – 10nm)

➢ **<u>Operation of MOSFET</u>**

- $v_{GS} = 0V$
  - No channel is created.
  - When a positive v_{DS} is applied no current flows from Drain to Source.
- Creating a channel for current flow



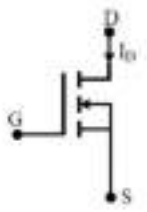
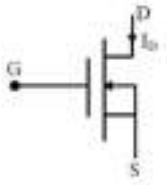
  - $v_{DS} = 0$ and a positive v_{GS} is applied at Gate.
  - +ve Gate voltage repels the holes near surface and creates a depletion region. As well, +ve Gate voltage attracts electrons from n+ Source and Drain.
  - An induced n region thus forms a channel for current flow from Drain to Source.
  - Hence the name n channel MOSFET or NMOS.
  - v_{GS} at which channel is formed is called threshold voltage v_t

  Now if positive v_{DS} is applied, electrons will move from Source to Drain along the channel. Thus, drain current flows from Drain to Source

➢ **<u>Why MOSFET?</u>**

- Gate – Oxide – Channel forms the MOS Capacitor.
- Gate turns the transistor (inversion layer) ON and OFF with an electric field through the oxide.

➢ **<u>Enhancement and depletion NMOS:</u>**

Enhancement type	**Depletion Type**
No channel at $\boldsymbol{v_{gs} = 0}$	Channel present at $\boldsymbol{v_{gs} = 0}$
Normally Open switch	Normally closed switch
	
Channel is enhanced as $\boldsymbol{v_{gs}}$ is increased	v_{gs} is made -ve to eliminate the channel already present.

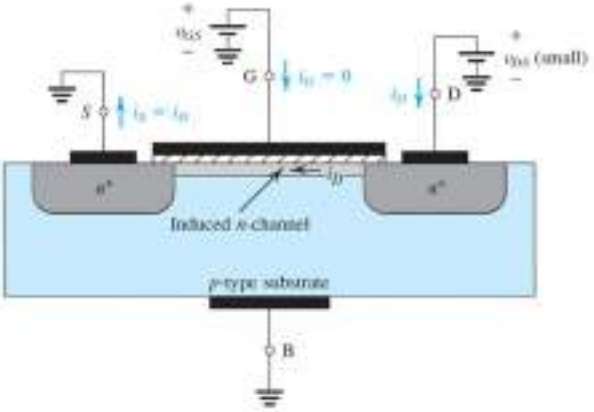
V – I Characteristics of MOSFET (n channel enhancement type)

- $v_{GS} = 0V$

  $i_D = 0$

- $v_{GS} > V_{TN}$ **and** v_{DS} **is increased.**

  - v_{DS} is very small



$$v_{OV} = v_{GS} - V_{TN}$$

$$|Q| = C_{OX}(WL)v_{OV}$$

$$\frac{|Q|}{L} = C_{OX}Wv_{OV}$$

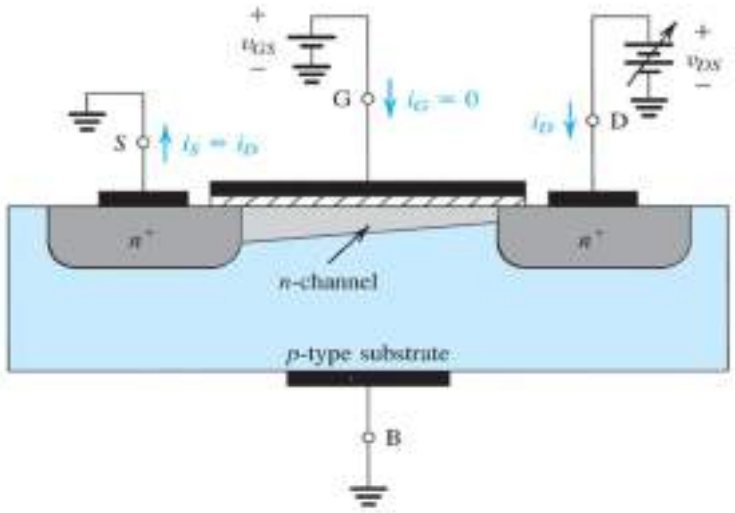
$$|E| = \frac{v_{DS}}{L}$$

$$v_d = \mu_n|E| = \mu_n \frac{v_{DS}}{L}$$

$$i_D = \left[(\mu_n C_{OX})\left(\frac{W}{L}\right)v_{OV}\right]v_{DS}$$

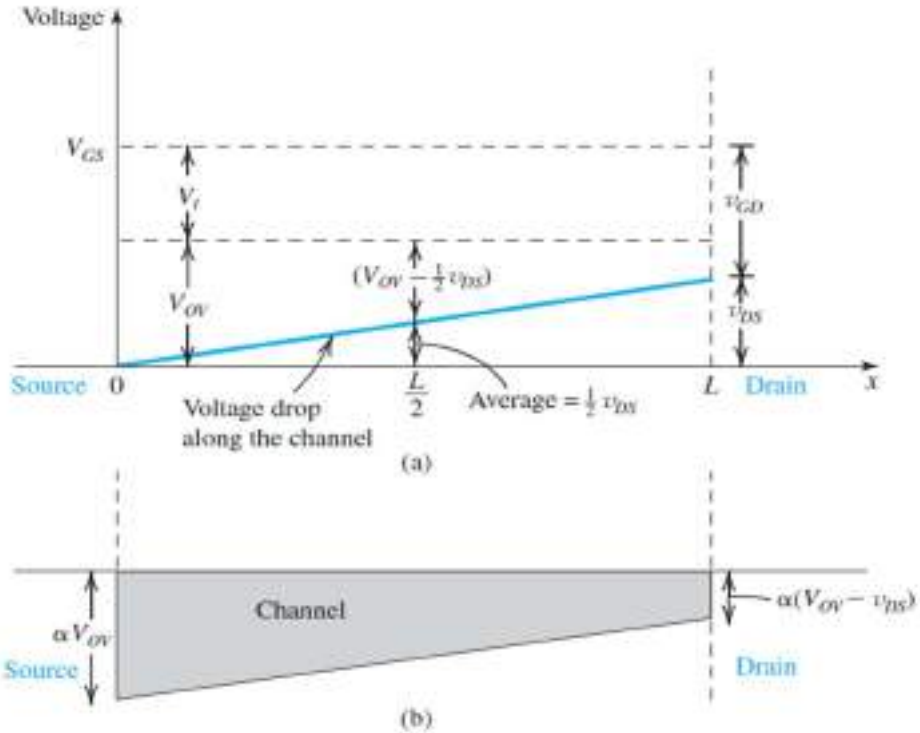
$$\Rightarrow i_D = \left[(\mu_n C_{OX})\left(\frac{W}{L}\right)(v_{GS} - V_{TN})\right]v_{DS}$$

- **As v_{DS} is increased $(v_{DS} < v_{OV})$**



$$v_{GS} = V_t + V_{OV}$$

$$v_{GD} = V_t + V_{OV} - v_{DS}$$



Charge in tapered channel is $\propto \frac{1}{2}[v_{OV} + (v_{OV} - v_{DS})]$

$$i_D = \left[(\mu_n C_{OX})\left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)\right]v_{DS}$$

$$\Rightarrow i_D = (\mu_n C_{OX})\left(\frac{W}{L}\right)\left(v_{OV}v_{DS} - \frac{1}{2}{v_{DS}}^2\right)$$

$$\Rightarrow \boldsymbol{i_D = (\mu_n C_{OX})\left(\frac{W}{L}\right)\left((v_{GS} - V_t)v_{DS} - \frac{1}{2}{v_{DS}}^2\right)}$$

- $\boldsymbol{v_{DS} \geq v_{OV}}$

  At $\boldsymbol{v_{DS} = v_{OV}}$, $\boldsymbol{v_{GD} = V_t}$, channel is **pinched off** at drain end. Increasing $\boldsymbol{v_{DS}}$ beyond v_{OV} has no effect on channel shape. Current is saturated**.**

$$\boldsymbol{v_{DS} = v_{OV} \Longrightarrow v_{DSATN} = v_{GS} - V_{TN}}$$

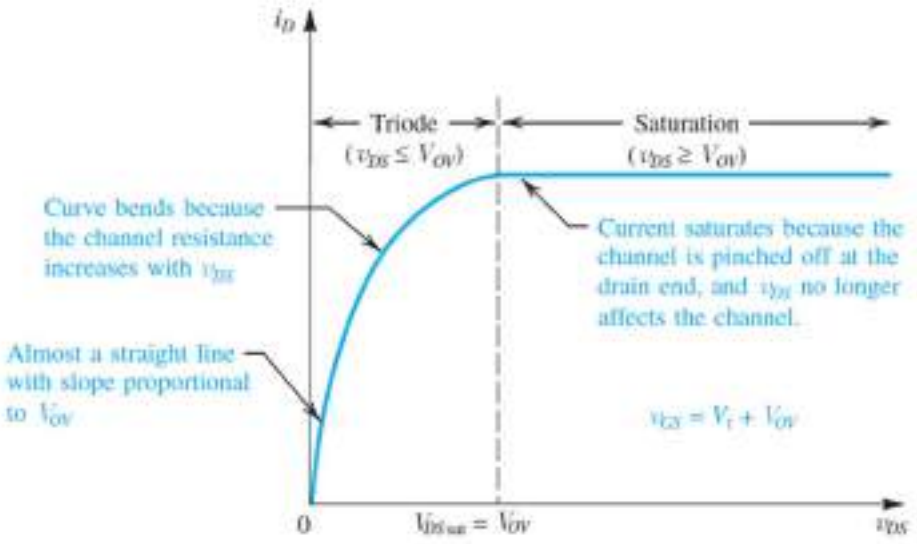
$$\boldsymbol{i_D = \frac{1}{2}(\mu_n C_{OX})\left(\frac{W}{L}\right)({v_{OV}}^2)}$$

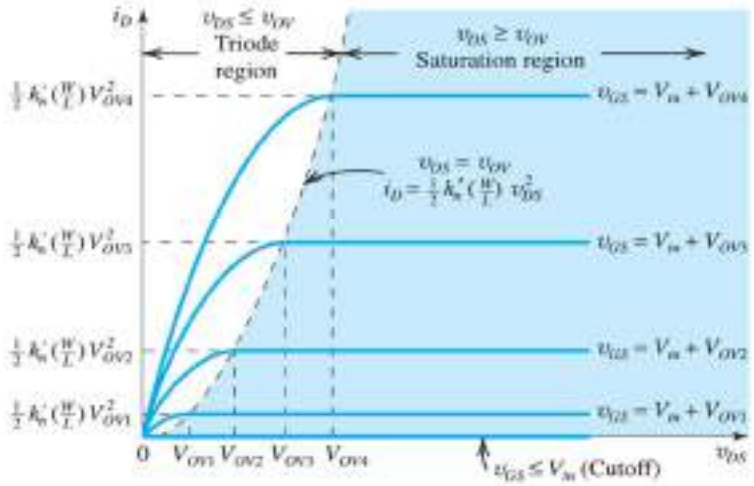
$$\boldsymbol{\Rightarrow i_D = \frac{1}{2}(\mu_n C_{OX})\left(\frac{W}{L}\right)(v_{GS} - V_{TN})^2}$$

- Process transconductance.

$$k'_n = \boldsymbol{\mu_n C_{OX}}$$

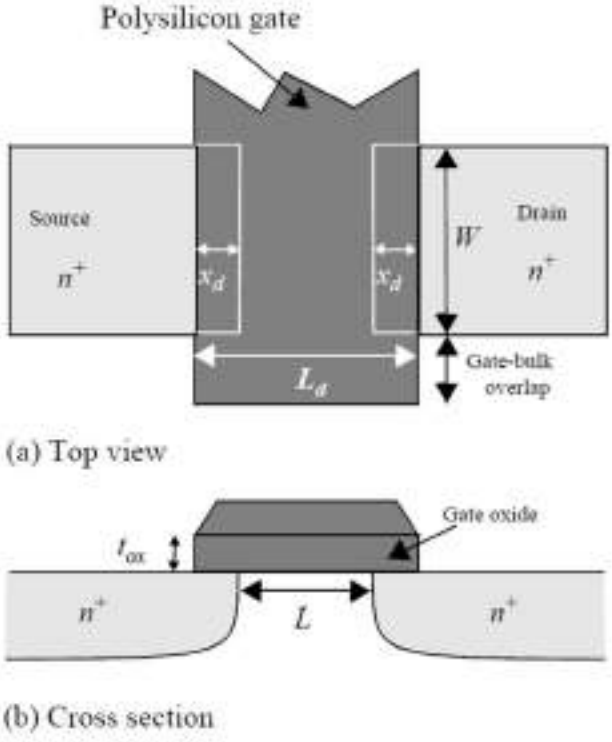
- MOSFET Transconductance, $\boldsymbol{k_n = k'_n\left(\frac{W}{L}\right) = \mu_n C_{OX}\left(\frac{W}{L}\right)}$
- $\boldsymbol{i_D}$ vs $\boldsymbol{v_{DS}}$ characteristics





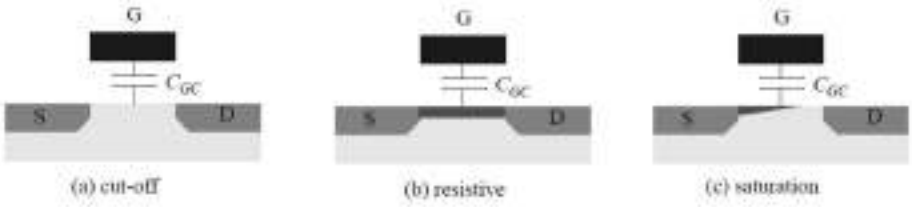
MOSFET Capacitances

- The dynamic response of a MOSFET transistor is a function of
  I. Time taken to charge (discharge) the parasitic capacitances that are intrinsic to the device
  II. The extra capacitance introduced by interconnecting lines
- The intrinsic (or parasitic capacitances) originate from three sources
  I. MOS structure
  II. Channel charge
  III. Depletion regions of the reversed biased PN-junctions of drain and source
- **MOS structure & Channel Charge**



- **C_G due to structure**
  Gate oxide capacitance per unit area, $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$.

  Source and drain have lateral diffusion of $\boldsymbol{x_d}$
  Effective channel length, $\boldsymbol{L = L_d - 2x_d}$
  Gate – Source and Gate – Drain overlap capacitances:
  $\boldsymbol{C_{GSO} = C_{GDO} = C_{ox}Wx_d = C_OW}$
- **C_G contributing to channel charge**



$$C_{GC} = C_{GCB} + C_{GCS} + C_{GCD}$$

$$C_G = C_{GC} + C_{GSO} + C_{GDO}$$

$$C_G = C_{GCB} + C_{GCS} + C_{GCD} + C_{GSO} + C_{GDO}$$

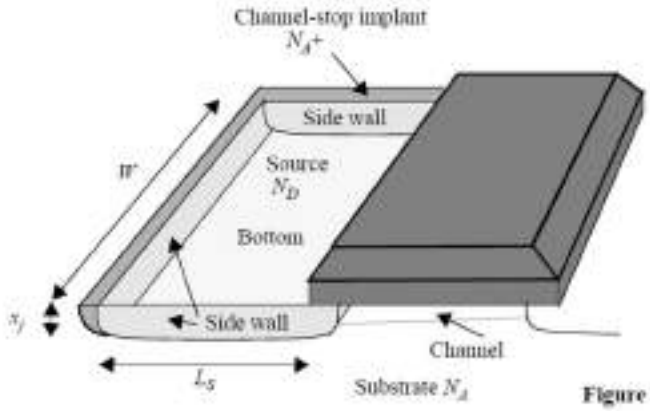
$$C_G = C_{GCB} + (C_{GCS} + C_{GSO}) + (C_{GCD} + C_{GDO})$$

$$C_G = C_{GB} + C_{GS} + C_{GD}$$

Operation Region	C_{GCB}	C_{GCS}	C_{GCD}	C_{GC}	C_G
Cutoff	$C_{ox}WL$	0	0	$C_{ox}WL$	$C_{ox}WL+2C_gW$
Resistive	0	$C_{ox}WL/2$	$C_{ox}WL/2$	$C_{ox}WL$	$C_{ox}WL+2C_gW$
Saturation	0	$(2/3)C_{ox}WL$	0	$(2/3)C_{ox}WL$	$(2/3)C_{ox}WL+2C_gW$

- **Junction Capacitances**

  Junction capacitance (often called diffusion capacitance) is contributed by reverse biased Source – Body and Drain – Body PN-junctions



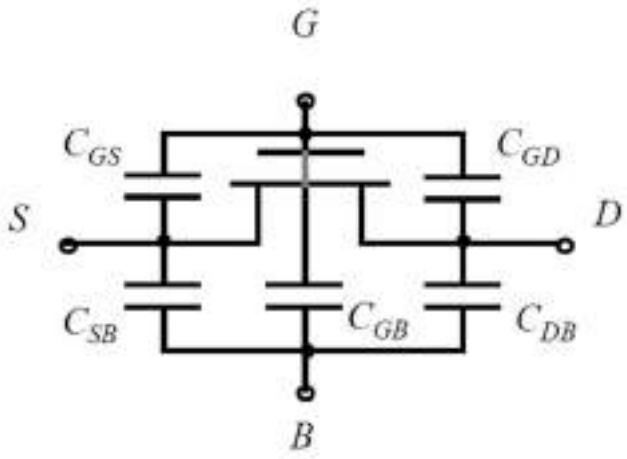
Figure

Bottom plate junction is formed by Source (Drain) and substrate. The side wall junction is formed by source (Drain) region and the channel stop implant

$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$
$$= C_j \times L_S \times W + C_{jsw} \times (2L_S + W)$$

C_j: Capacitance per unit area

C_jsw: Capacitance per unit perimeter


G
C_{GS}
C_{GD}
S
D
C_{SB}
C_{GB}
C_{DB}
B

Modelling of MOS transistor – SPICE Levels: 1,2,3

- SPICE has 3 built in MOSFET models.
- All these models are now obsolete (due to short channel devices)
- All these models are limited to first order analysis.
    - LEVEL1 SPICE
    - LEVEL2 SPICE
    - LEVEL3 SPICE
- **SPICE Level 1**
    - Implements the ***Shichman – Hodges*** model based on long channel square law expression. It is closely related to **Shockley model** with **channel length modulation** and the **body effect**.
    - It does **NOT** handle **short – channel** effects.

$$i_D = \begin{cases} \mathbf{0}, & v_{GS} < V_{TN} \quad cutoff \\ (KP)\left(\frac{W_{eff}}{L_{eff}}\right)(1 + LAMBDA\, v_{DS})\left((v_{GS} - V_t) - \frac{1}{2}v_{DS}\right), & v_{DS} < v_{GS} - V_{TN} \quad linear \\ \left(\frac{KP}{2}\right)\left(\frac{W_{eff}}{L_{eff}}\right)(1 + LAMBDA\, v_{DS})(v_{GS} - V_{TN})^2, & v_{DS} \geq v_{GS} - V_{TN} \quad saturation \end{cases}$$

- Parameters from SPICE are in ALL CAPS.

  $\boldsymbol{k_n} = (KP)\left(\frac{W_{eff}}{L_{eff}}\right)$

  $\boldsymbol{k_n'} = \boldsymbol{KP}$

  $\boldsymbol{LAMBDA} = \frac{1}{V_A} = \boldsymbol{\lambda}$ **,** it accounts for the channel length modulation

  The threshold voltage is modulated by $\boldsymbol{v_{SB}}$ (non – negative) through the body effect.

  $\boldsymbol{V_{TN} = VTO + GAMMA}\left(\sqrt{\boldsymbol{PHI} + \boldsymbol{v_{SB}}} - \sqrt{\boldsymbol{PHI}}\right)$

  $\boldsymbol{VTO}$ is the zero bias threshold voltage V_{TNO}

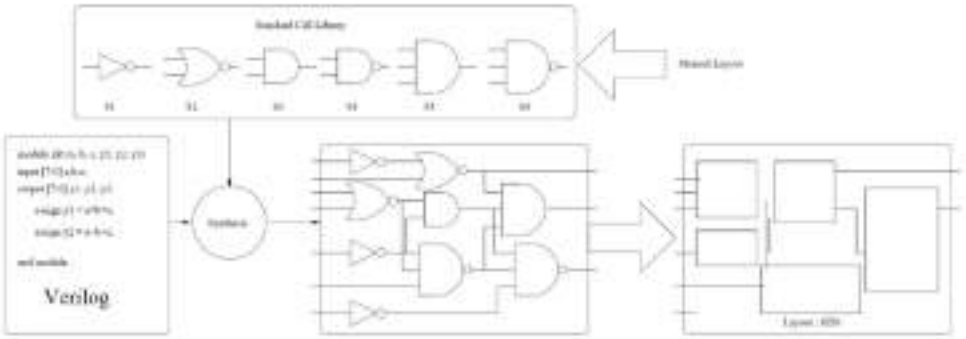
  $\boldsymbol{PHI}$ is the surface potential $\boldsymbol{\phi_s}$

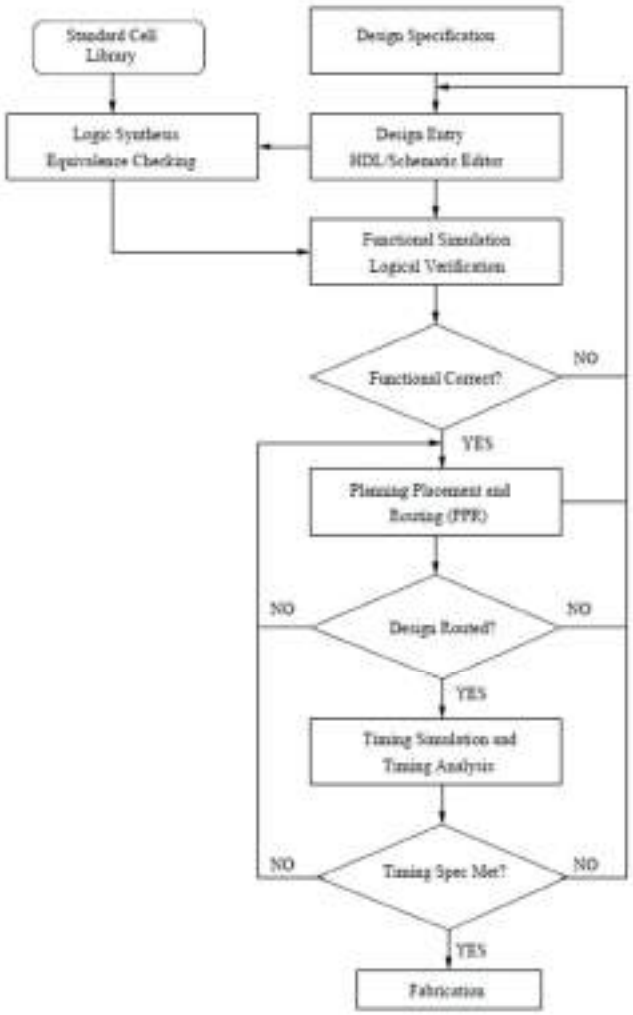
  $\boldsymbol{GAMMA}$ is the body effect coefficient $\boldsymbol{\gamma}$

  $\boldsymbol{TOX}$ is the oxide thickness $\boldsymbol{t_{OX}}$
- **LEVEL 1 SPICE** model also includes parameters to compute the diffusion capacitance.
- **SPICE Level 2**
    - Geometry – based model, uses detailed device physics to define its equations.
    - It handles such as: velocity saturation, mobility degradation, drain induced barrier lowering (DIBL).
- **SPICE Level 3**
    - A semi empirical model.
    - Works quite well for channel length down to 1µm.

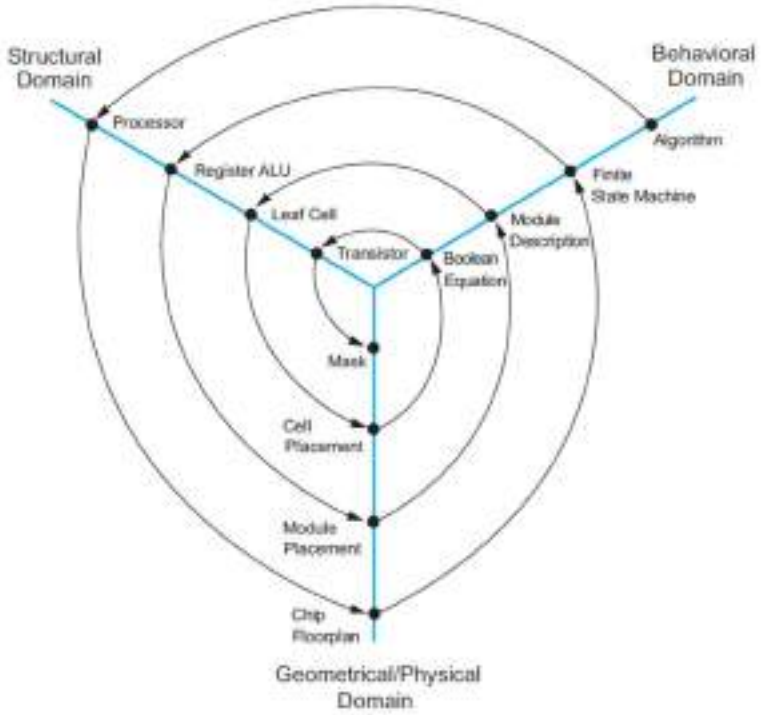
VLSI Design Flow

- Chip design is heavily automated.
- Only critical blocks are hand laid out.
- Significant portion of the chip is described using Hardware Description Language (HDL)
- Only standard cells are laid out manually
- Analog blocks are custom designed - Heavily layout sensitive
- Push button level automation is available





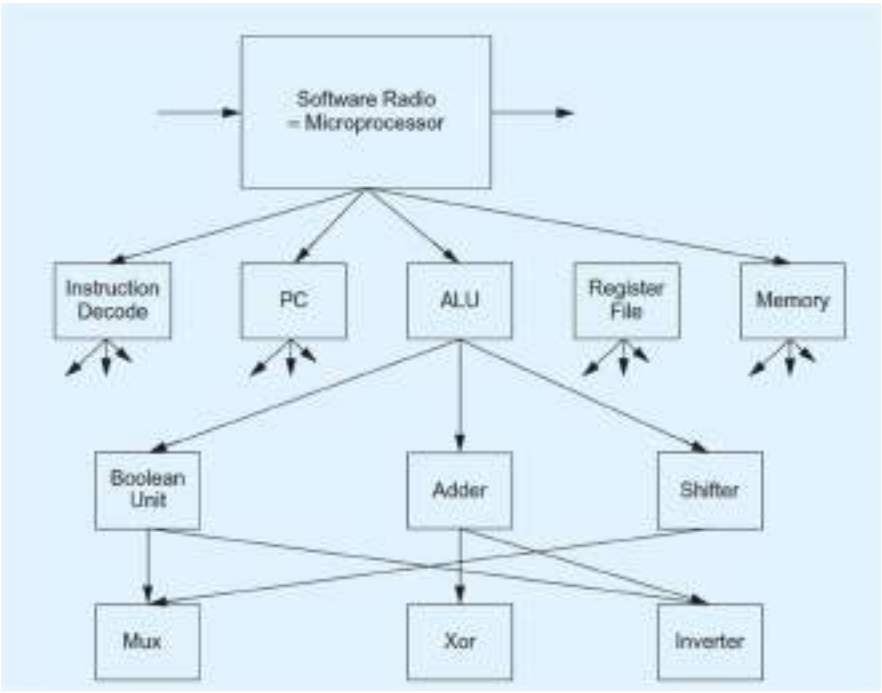
Y – Chart



- The Y chart consists of 3 domains of representation
    a. **Behavioural Domain**
    b. **Structural Domain**
    c. **Physical/Geometrical Domain**
- Within each domain there are a number of design abstractions that starts at a high level and descends to the individual elements that need to be aggregated to yield the top-level function.
- **Behavioural domain** describes what a particular system does.
- **Structural domain** describes the interconnection of modules necessary to achieve a particular behaviour.
- **Physical domain** description explains how to physically construct that level of abstraction.
    I. The design flow starts from the **algorithm** that describes the behaviour of target chip. The corresponding architecture of the **processor** is first defined. It is mapped onto chip surface by **floor planning.**
    II. The next design evolution in the behavioural domain defines FSM (**finite state machine**) which are structurally implemented with functional modules such as **Registers and ALUs**. These modules are then geometrically placed onto chip surface using CAD tools for automatic **module placement** followed by routing to minimize interconnect area and signal delays
    III. The third evolution starts with a behavioural **model description**. Individual modules are then implemented with **leaf cells**. At this stage the chip is described in terms of logic gates (leaf cells), which can be placed and interconnected by using a **cell placement** and routing program.
    IV. The last evolution involves a detailed **Boolean description** of leaf cells followed by a **transistor level** implementation of leaf cells and **mask generation**

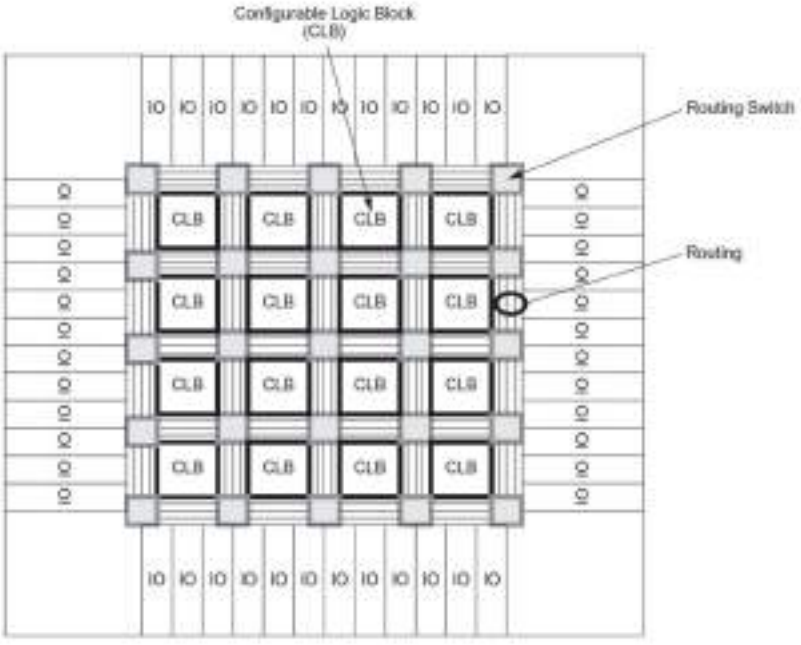
Design Hierarchy

- The use of hierarchy involves dividing a module into sub modules and so on until the smaller parts become manageable.
- VLSI design flow (Y chart) consists of 3 domains of representations. A hierarchy structure can be described in each of these domains.
- **Parallel Hierarchy:** Hierarchies in different domains can be mapped into each other easily.
- Equivalency can ensure the consistency of each domain. These tools can be applied hierarchically checking each level of hierarchy where domains are intended to correspond.
- **Example**:
    - A RISC processor core can have an HDL model that describes the behaviour of the processor.
    - A Gate Netlist that describes the type and interconnection of gates required to produce the processor.
    - A placement and routing description describes how physically build the processor in given process.
- Hierarchy allows the use of virtual components. (Soft versions of the more conventional packaged IC)
- Virtual components are placed into a chip design as pieces of code and come with support documentation such as verification scripts.
- Example:
    - Microprocessor, here is the basis for design of software radio.
    - The design might have the hierarchy of a typical microprocessor.
    - At the top-level Microprocessor contains an ALU (Arithmetic Logic Unit), PC (Program Counter), Register File, ID (Instruction Decoder), and Memory.
    - The ALU may be further decomposed into an Adder, A Boolean Logic Unit and a Shifter.
    - The Shifter and the Adder can together can together perform addition.

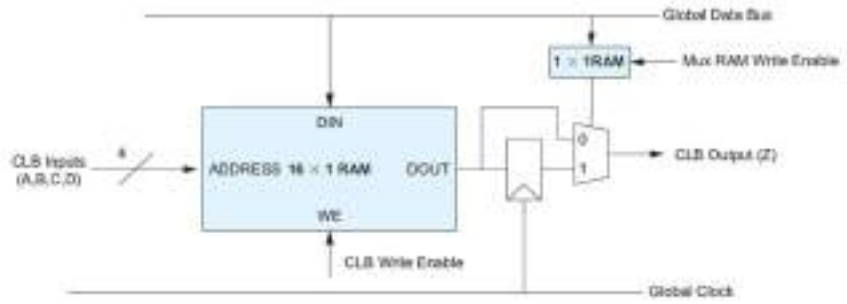


VLSI design methodologies

- Some of the VLSI design methodologies are
  - Microprocessor/DSP
  - PLD (Programmable Logic devices)
  - FPGA (Field Programmable Gate Arrays)
  - Cell-based
  - Custom design
  - Platform based
- PLD:
  - Based on PLAs.
  - A PLA consists of an AND plane and an OR plane to compute any function expressed as SOP.
  - NOR structure at PLA locations allows each transistor in the AND & OR plane programmed to be present or not.
  - PLDs have limited routing capabilities.
  - Each node is programmed with a floating gate transistor, a fusible link or a RAM – controlled transistor.
- FPGA
  - Use high circuit densities to construct ICs.
  - FPGAs are completely programmable even after a product is shipped or "in the field".
  - Two basic versions of FPGAs exist.
    I. The first uses fuse or antifuse to permanently program interconnect and personalise logic.
    II. The second type uses Static RAM or Flash Memory to configure routing and logic functions
  - In general, an FPGA chip consists of an array of logic cells surrounded by programmable routing resources.
  -



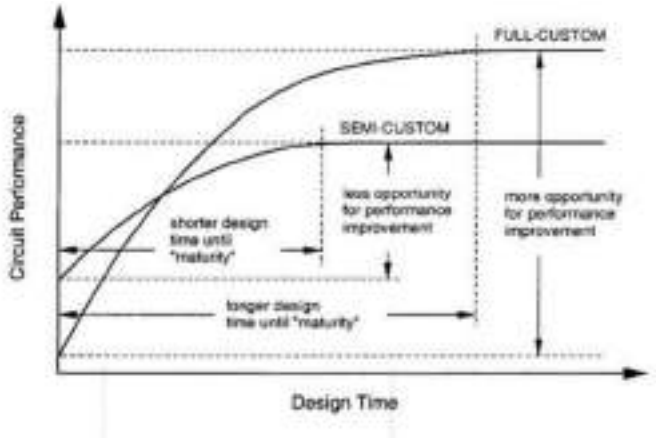
I. Above figure shows the floor plan of a simplified FPFA.
II. The chip is composed of an array of Configurable Logic Blocks (CLBs).
III. Metal routing tracks run vertically and horizontally between the array of CLBs
IV. Metal routing tracks terminate at routing switches that can be implemented using antifuse, CMOS transmission gates or tristate buffers.
V. Routing resources can also be connected to inputs and outputs of adjacent CLBs.
VI. CLBs use programmable look up tables to compute any function of several variables.
VII. Configurable IO cells that can be used as input, output, or bidirectional pads surround the core array of CLBs.
VIII. A simplified SRAM based FPGA logic cell is shown below.



- Cell based design
  - Cell based design uses a standard cell library as the building blocks of a chip.
  - Cells with wide range of functionalities are available.
  - Example
    - SSI logic (NAND, NOR, XOR, AOI, OAI, Inverters, Buffers, Registers)
    - Memories (RAM, ROM, CAM, Register Files)
    - System level modules (processors, protocol processors, serial interfaces, bus interfaces)
    - Possibility of mixed signal and RF modules.
- Custom design (Full Custom design).
  - Oldest and most traditional technique to design standard cells or larger circuit blocks.
- Platform based design – System on a chip
  - Use of predefined IP blocks (such as RISC processors, memory and IO functions attached to the common buses)
  - A platform can be used implement a design by using buses and high-level programming languages (like C).
  - Platform based system consists of a basic RISC processor which can be extended with multipliers, floating point units, or specialised DSP units.

Design Method	Non-Recurring Engineering	Unit Cost	Power Dissipation	Complexity of Implementation	Time to Market	Performance	Flexibility
Microprocessor/DSP	Low	Medium	High	Low	Low	Low	High
PLD	Low	Medium	Medium	Low	Low	Medium	Low
FPGA	Low	Medium	Medium	Medium	Low	High	High
Cell-Based	High	Low	Low	High	High	High	Low
Custom Design	High	Low	Low	High	High	Very High	Low
Platform-Based	High	Low	Low	High	High	High	Medium

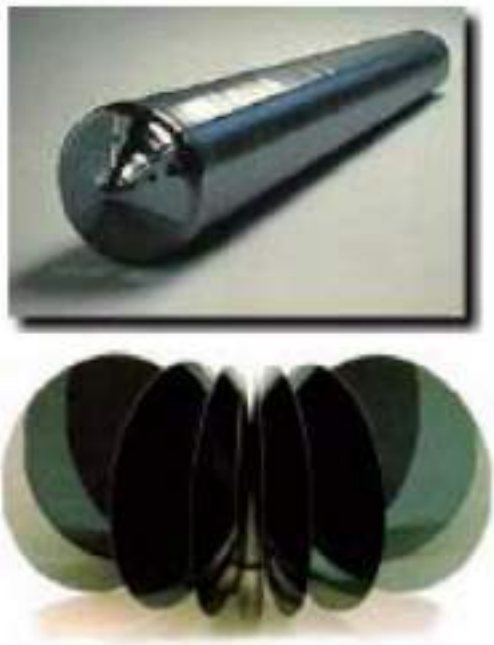
- Full Custom vs Semicustom



Full Custom Design	**Semi-Custom Design**
Placement and geometry of every transistor can be optimized individually.	It uses standard cell-based design or FPGA.
It requires longer design time until maturity.	It requires shorter design time until maturity.
Design is more flexible	Design is less flexible
It has more opportunity for performance improvement	It has less opportunity for performance improvement
Performance is High (High Speed, Low Power dissipation)	Performance is Low (Low Speed, High Power dissipation)
Design Complexity is more	Design Complexity is less
High cost	Low cost
Highly compact	Less compact
Example – Microprocessor	Example – Digital Logics

Basic IC Fabrication Steps

- The CMOS process requires a large number of steps, each of which consists of a sequence of basic operations. A number of these steps and/or operations are executed very repetitively in the course of the manufacturing process.
  - **The Silicon Wafer**
    I. The base material for the manufacturing process comes in the form of a single-crystalline, lightly doped *wafer*.
    II. These wafers have typical diameters between 4 and 12 inches (10 and 30 cm, respectively) and a thickness of at most 1 mm, and are obtained by cutting a single crystal ingot into thin slices.
    III. A starting wafer of the *p*-type might be doped around the levels of $2 \times 10^{21} impurities/m^3$.
    IV. Often, the surface of the wafer is doped more heavily, and a single crystal *epitaxial layer* of the opposite type is grown over the surface before the wafers are handed to the processing company.
    V. One important metric is the **defect density** of the base material. High defect densities lead to a larger fraction of non- functional circuits, and consequently an increase in cost of the final product.



  - **Photolithography**
    I. The technique to accomplish selective masking is called photolithography.
    II. In each processing step, a certain area on chip is masked out using the appropriate optical mask so that a desired processing step can be selectively applied to the remaining regions.
    III. The processing steps may be **oxidation, etching, metal and Polysilicon deposition, ion implantation.**

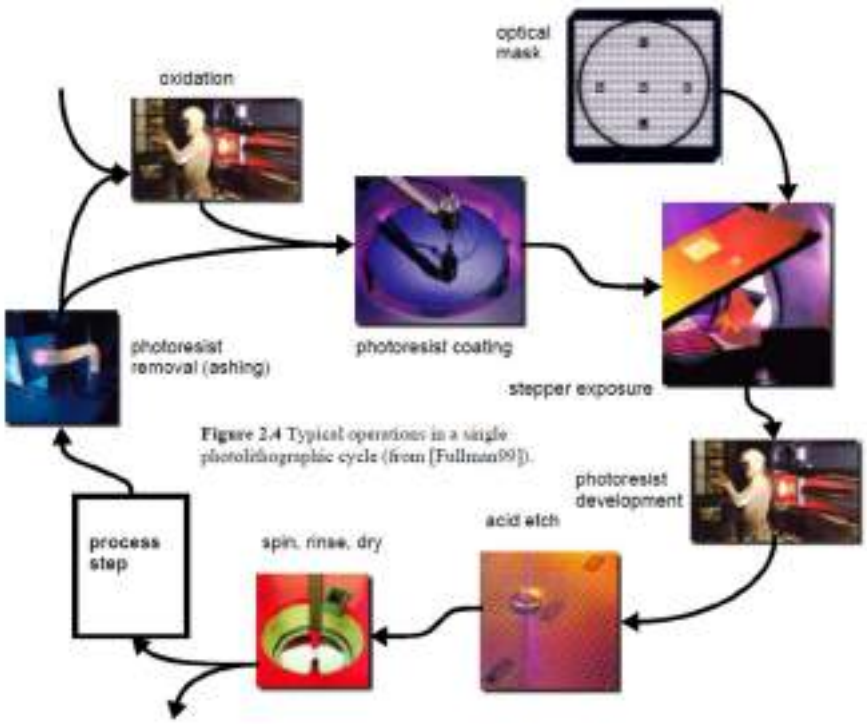


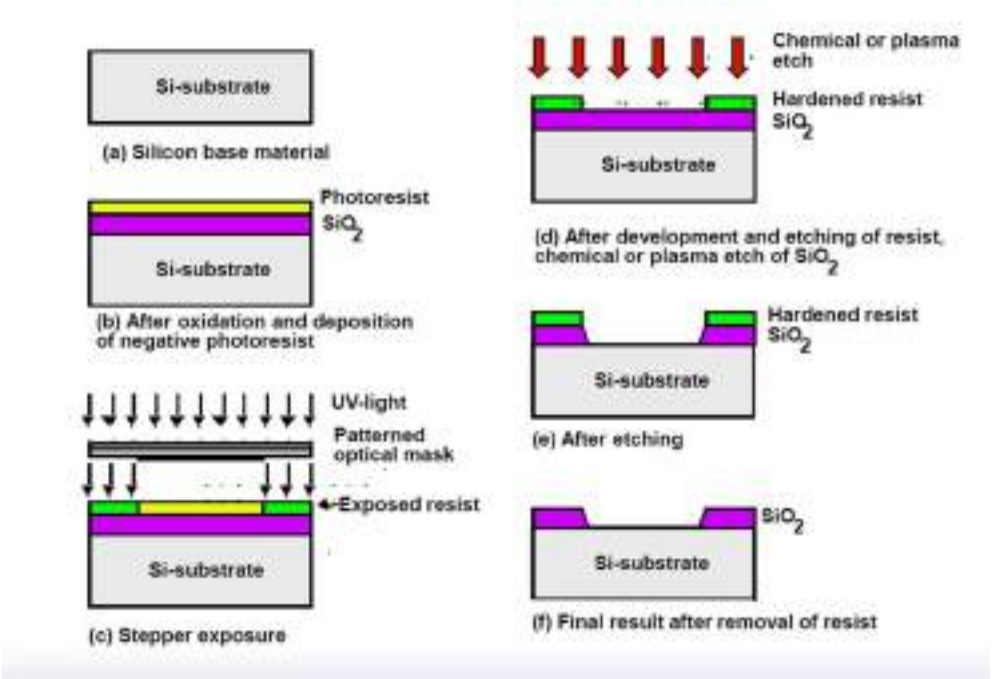
Figure 2.4 Typical operations in a single photolithographic cycle (from [Fullman99]).

- ***Oxidation layering*:**
  This optional step deposits a thin layer of SiO_2 over the complete wafer by exposing it to a mixture of high-purity oxygen and hydrogen at approximately 1000°C. The oxide is used as an insulation layer and also forms transistor gates.
- ***Photoresist coating***
  A light-sensitive polymer (similar to latex) is evenly applied while spinning the wafer to a thickness of approximately 1 mm. This material is originally soluble in an organic solvent, but has the property that the polymers cross link when exposed to light, making the affected regions insoluble. A photoresist of this type is called *negative*. A positive photoresist has the opposite properties; originally insoluble, but soluble after exposure. By using both positive and negative resists, a single mask can sometimes be used for two steps, making complementary regions available for processing.
- ***Stepper exposure***
  A glass mask (or reticle), containing the patterns that we want to transfer to the silicon, is brought in close proximity to the wafer. The mask is opaque in the regions that we want to process, and transparent in the others (assuming a negative photoresist). The combination of mask and wafer is now exposed to ultra-violet light. Where the mask is transparent, the photoresist becomes insoluble.
- ***Photoresist development and bake***
  The wafers are developed in either an acid or base solution to remove the non-exposed areas of photoresist. Once the exposed photoresist is removed, the wafer is “soft-baked” at a low temperature to harden the remaining photoresist.
- ***Acid Etching***
  Material is selectively removed from areas of the wafer that are not covered by photoresist. This is accomplished through the use of many different types of acid, base and caustic solutions as a function of the material that is to be removed. Much of the work with chemicals takes place at large wet benches where special solutions are prepared for specific tasks. Because of the dangerous nature of some of these solvents, safety and environmental impact is a primary concern.
- ***Spin, rinse, and dry***

Special tool (called SRD) cleans the wafer with deionized water and dries it with nitrogen. The microscopic scale of modern semiconductor devices means that even the smallest particle of dust or dirt can destroy the circuitry. To prevent this from happening, the processing steps are performed in ultra-clean rooms where the number of dust particles per cubic foot of air ranges between 1 and 10. Automatic wafer handling and robotics are used whenever possible. This explains why the cost of a state-of-the-art fabrication facility easily ranges in the multiple billions of dollars. Even then, the wafers must be constantly cleaned to avoid contamination, and to remove the left-over of the previous process steps.

- ***Various process steps***
  The exposed area can now be subjected to a wide range of process steps, such as ion implantation, plasma etching, or metal deposition.
- ***Photoresist removal (or ashing)***
  A high-temperature plasma is used to selectively remove the remaining photoresist without damaging device layers.

➢ **Process Steps for patterning SiO_2 layer**



➢ **Some recurring process steps**

- **Diffusion and ion implantation**

  There exist two approaches for introducing these dopants – diffusion and ion implantation. The creation of the source and drain regions, well and substrate contacts, the doping of the polysilicon, and the adjustments of
  the device threshold requires diffusion and ion implantation.

  - ***Diffusion implantation***
    In *diffusion implantation*, the wafers are placed in a quartz tube embedded in a heated furnace. A gas containing the dopant is introduced in the tube. The high temperatures of the furnace, typically 900 to 1100 °C, cause the dopants to diffuse into the exposed surface both vertically and horizontally. The final dopant concentration is the greatest at the surface and decreases in a gaussian profile deeper in the material.
  - ***Ion implantation***
    In *ion implantation*, dopants are introduced as ions into the material. The ion implantation system directs and sweeps a beam of purified ions over the semiconductor surface. The acceleration of the ions determines how deep they will penetrate the material, while the beam current and the exposure time determine the

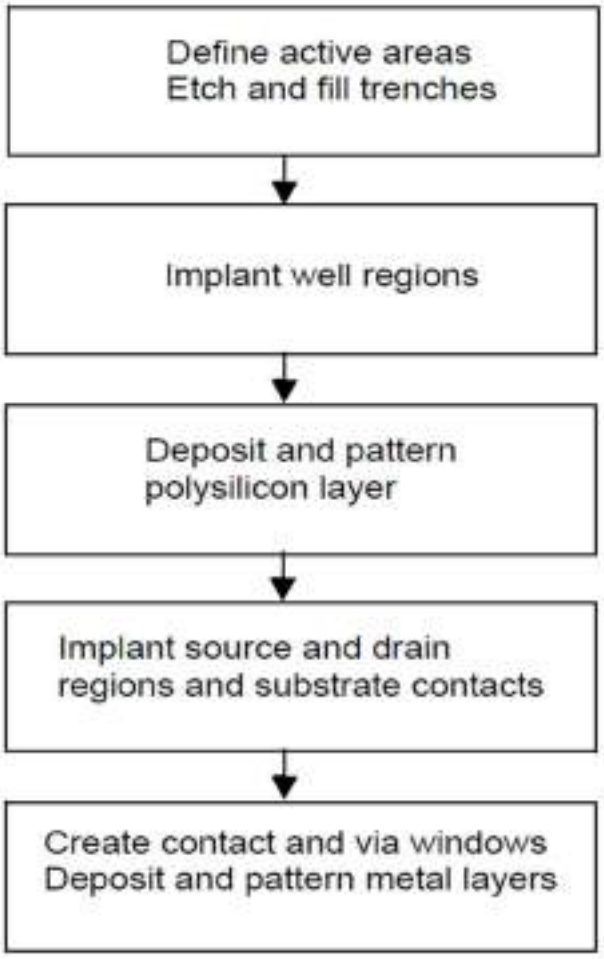
dosage. The ion implantation method allows for an independent control of depth and dosage. This is the reason that ion implantation has largely displaced diffusion in modern semiconductor manufacturing.

Ion implantation has some unfortunate side effects however, the most important one being lattice damage. Nuclear collisions during the high energy implantation cause the displacement of substrate atoms, leading to material defects. This problem is largely resolved by applying a subsequent *annealing* step, in which the wafer is heated to around 1000°C for 15 to 30 minutes, and then allowed to cool slowly. The heating step thermally vibrates the atoms, which allows the bonds to reform.

- **Deposition**
  Any CMOS process requires the repetitive deposition of layers of a material over the complete wafer, to either act as buffers for a processing step, or as insulating or conducting layers.
  - **Silicon nitride** (Si_3N_4) is used as a sacrificial buffer material during the formation of the field oxide and the introduction of the stopper implants. This silicon nitride is deposited everywhere using a process called *chemical vapor deposition* or CVD, which uses a gas-phase reaction with energy supplied by heat at around 850°C.
  - **Polysilicon**, on the other hand, is deposited using a chemical deposition process, which flows silane gas over the heated wafer coated with SiO_2 at a temperature of approximately 650°C. The resulting reaction produces a non-crystalline or amorphous material called polysilicon. To increase to conductivity of the material, the deposition has to be followed by an implantation step.
  - The **Aluminium** interconnect layers are typically deployed using a process known as *sputtering*. The aluminium is evaporated in a vacuum, with the heat for the evaporation delivered by electron-beam or ion-beam bombarding.
- **Etching**
  Once a material has been deposited, etching is used to selectively form patterns such as wires and contact holes.

  - The ***wet etching*** process makes use of acid or basic solutions. For instance, hydrofluoric acid buffered with ammonium fluoride is typically used to etch SiO_2.
  - ***Dry* or *plasma etching***: A wafer is placed into the etch tool's processing chamber and given a negative electrical charge. The chamber is heated to 100°C and brought to a vacuum level of 7.5 Pa, then filled with a positively charged plasma (usually a mix of nitrogen, chlorine and boron trichloride). The opposing electrical charges cause the rapidly moving plasma molecules to align themselves in a vertical direction, forming a microscopic chemical and physical “sandblasting” action which removes the exposed material. Plasma etching has the advantage of offering a well-defined directionality to the etching action, creating patterns with sharp vertical contours.
- **Planarization**
  To reliably deposit a layer of material onto the semiconductor surface, it is essential that the surface is approximately flat. Therefore, a *chemical-mechanical planarization* (CMP) step is included before the deposition of an extra metal layer on top of the insulating SiO_2 layer. This process uses a slurry compound—a liquid carrier with a suspended abrasive component such as aluminium oxide or silica—to microscopically plane a device layer and to reduce the step heights

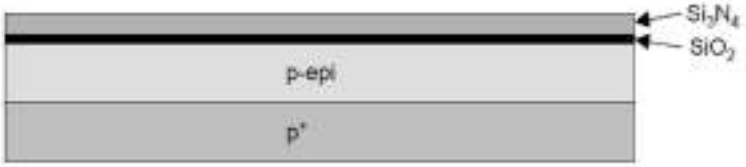
Simplified process sequence of CMOS



- The process starts with definition of active regions, where transistors will be constructed. All other areas of the die will be covered with SiO_2, called field oxide. This oxide acts as the insulator between neighbouring devices, and is either grown or deposited in etched trenches hence the name *trench insulation.* Further insulation is provided by the addition of a reverse-biased *np*-diode, formed by adding an extra p^+ region, called the *channel-stop implant* (or *field implant*) underneath the field oxide
- lightly doped *p*- and *n*-wells are formed through ion implantation. To construct an NMOS transistor in a *p*-well, heavily doped *n*-type *source* and *drain* regions are implanted (or diffused) into the lightly doped *p*-type substrate.
- A thin layer of SiO_2, called the *gate oxide*, separates the region between the source and drain, and is itself covered by conductive polycrystalline silicon (or polysilicon, for short). The conductive material forms the *gate* of the transistor.
- PMOS transistors are constructed in an *n*-well in a similar fashion (just reverse *n*'s and *p*'s).
- Multiple insulated layers of metallic (most often Aluminium) wires are deposited on top of these devices to provide for the necessary interconnections between the transistors

Fabrication process of a dual well CMOS circuit

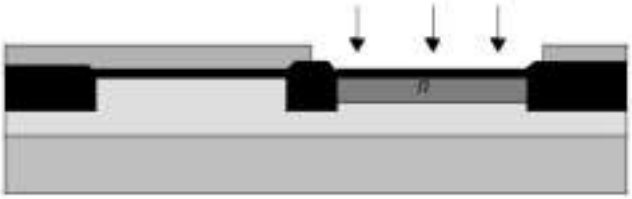
(a) Base material: p+ substrate with p-epi layer



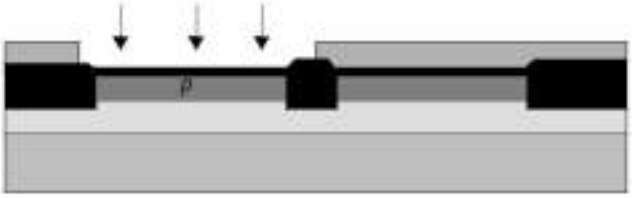
(b) After deposition of gate-oxide sacrificial nitride (acts as a buffer layer)

(c) After plasma etch of insulating trenches using the inverse of the active area mask

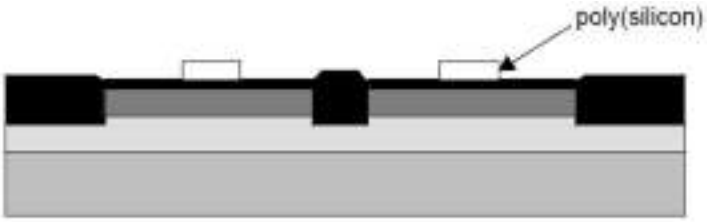
(d) After trench filling, CMP planarization, and removal of sacrificial nitride



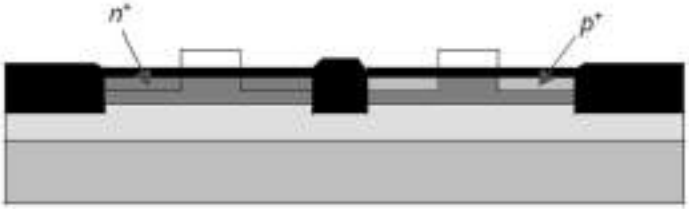
(e) After *n*-well and V_{Tp} adjust implants



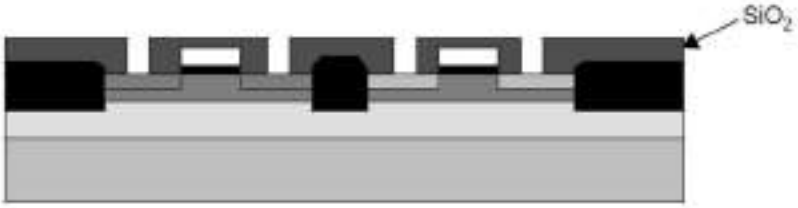
(f) After *p*-well and V_{Tn} adjust implants



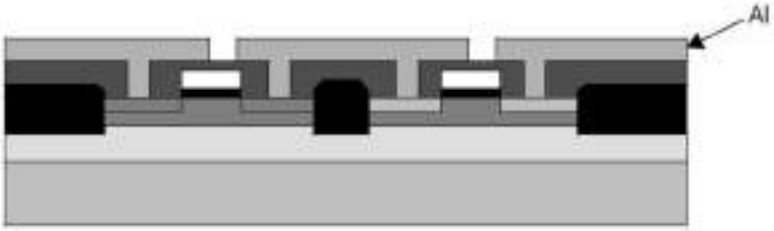
(g) After polysilicon deposition and etch



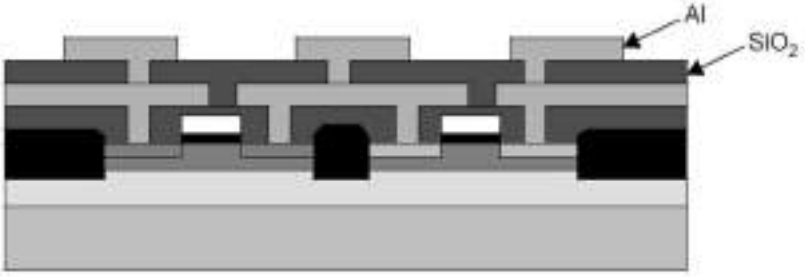
(h) After n^+ source/drain and p^+ source/drain implants. These steps also dope the polysilicon.



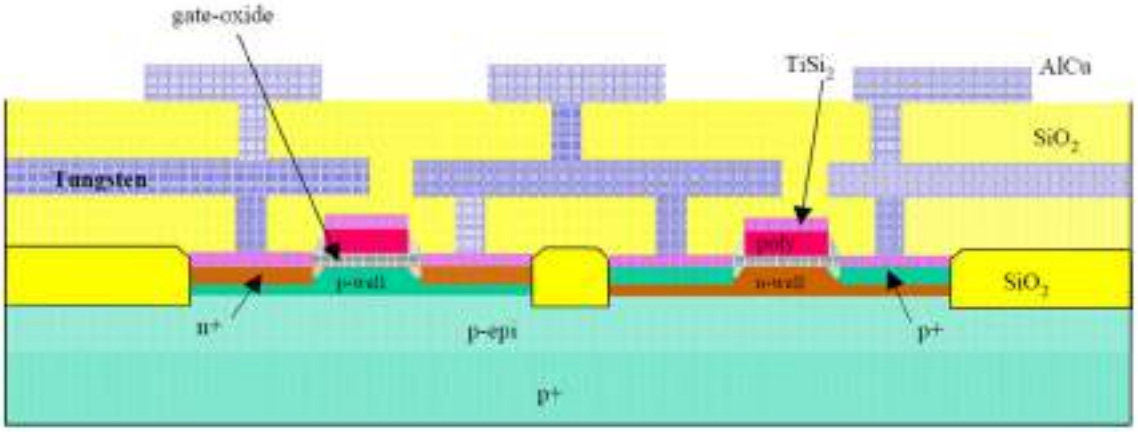
(i) After deposition of SiO_2 insulator and contact hole etch.



(j) After deposition and patterning of first Al layer.

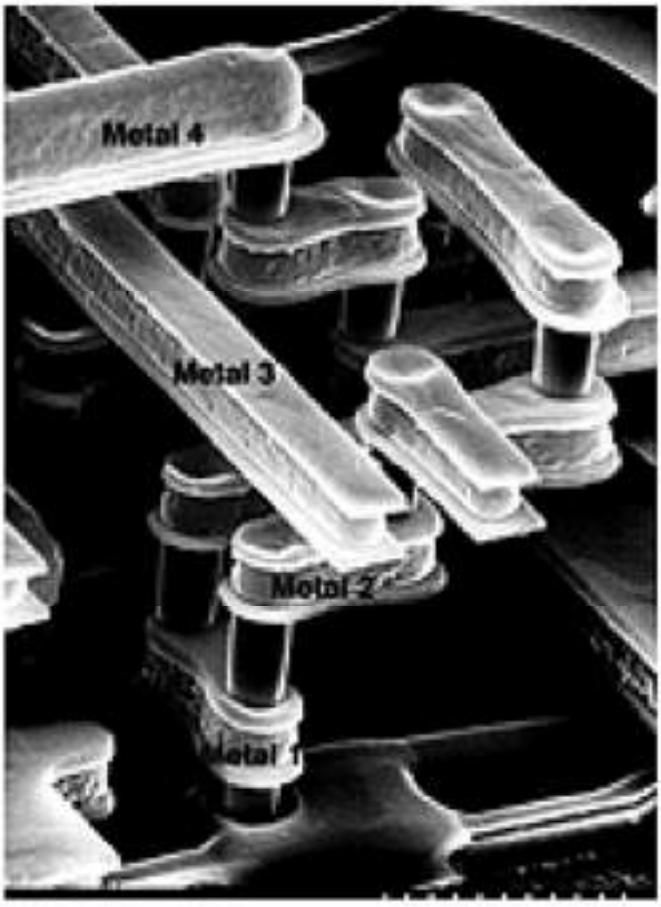


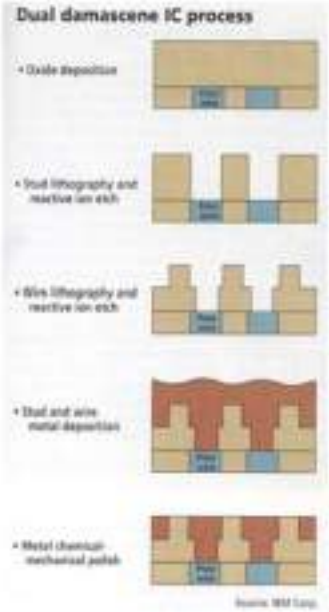
(k) After deposition of SiO_2 insulator, etching of via's, deposition and patterning of second layer of Al.

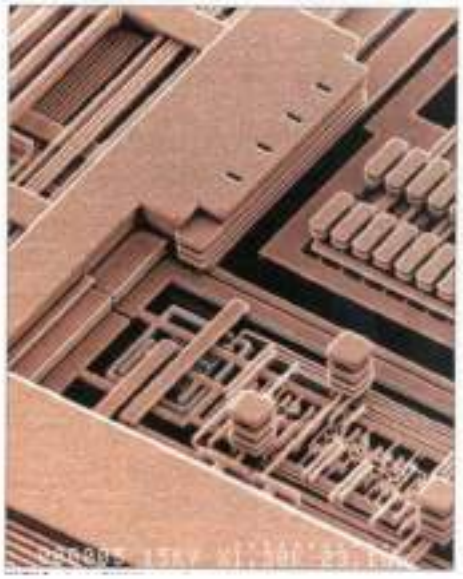


Dual-Well Trench-Isolated CMOS Process

- Advanced metallization




Dual damascene IC process
• Oxide deposition
• Stud lithography and reactive ion etch
• Wire lithography and reactive ion etch
• Stud and wire metal deposition
• Metal chemical-mechanical polish



Layout design rules

- **Design rules**
  - Interface between designer and process engineer.
  - Guidelines for constructing process mask.
  - Unit dimension: Minimum line width
    1. Scalable design rules – Lambda Parameter
    2. Absolute dimensions – Micron rules
- **Scalable design rule**
  - All rules are a function of single parameter λ
  - λ is the resolution of patterning process.
  - λ is half of the minimum line width (Polysilicon wire) or half of the transistor channel length.
  - Design is easily ported over a cross section of industrial processes by scaling λ. This results in a linear scaling of all dimensions.
  - Conservative

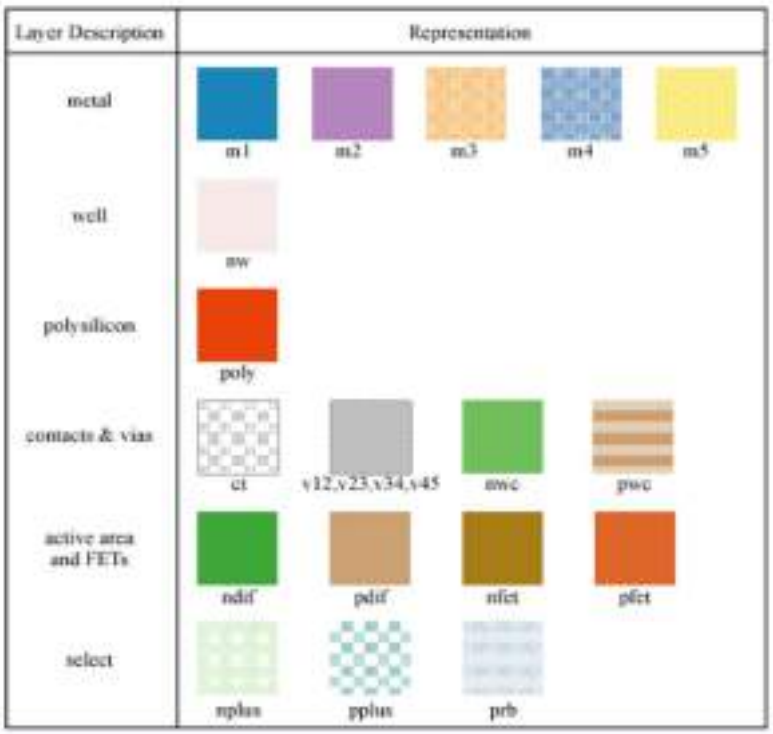
Example:
For a 0.25 µm process (i.e., minimum line width=0.25 µm)
Minimum line width = 2λ = minimum channel length
And λ=0.125 µm

- **Micron rule**
  - Design rules are expressed in absolute dimensions.
  - Aggressive

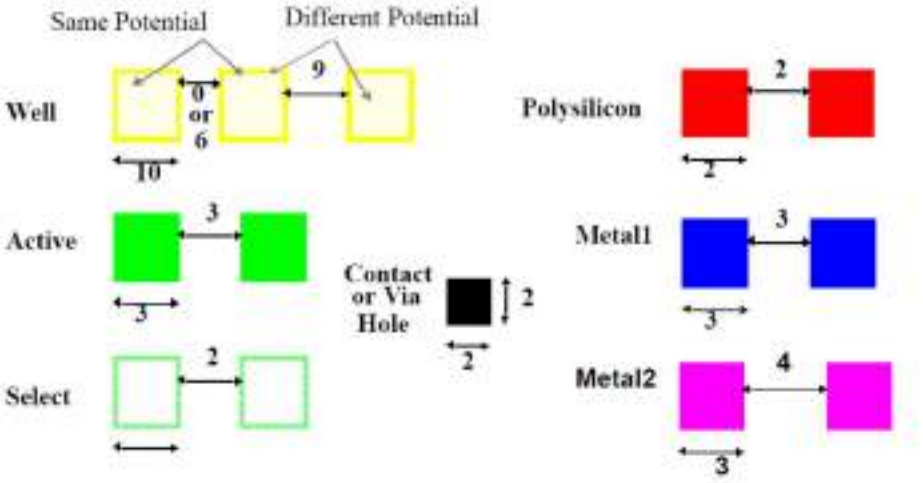
- CMOS Process layers:

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

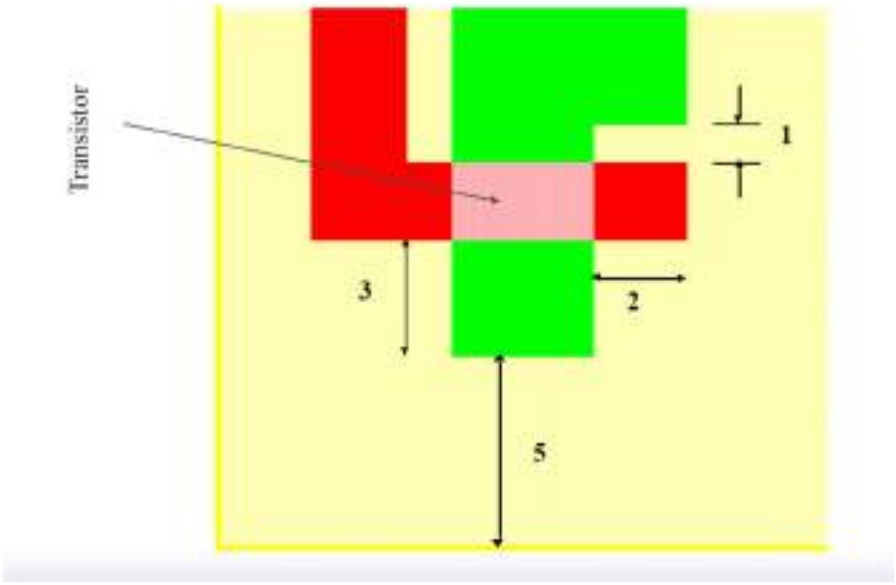
- Layers in 0.25 µm CMOS process



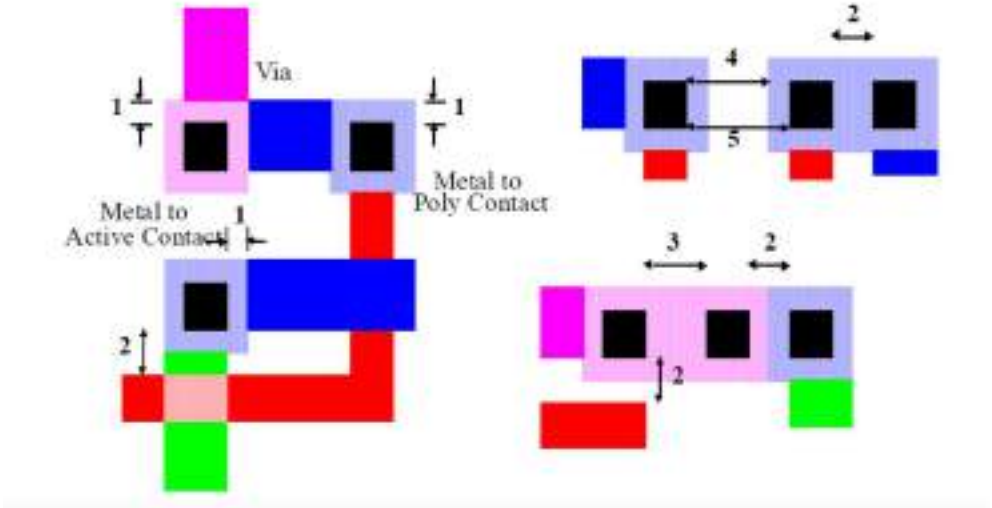
- Intra layer design rules



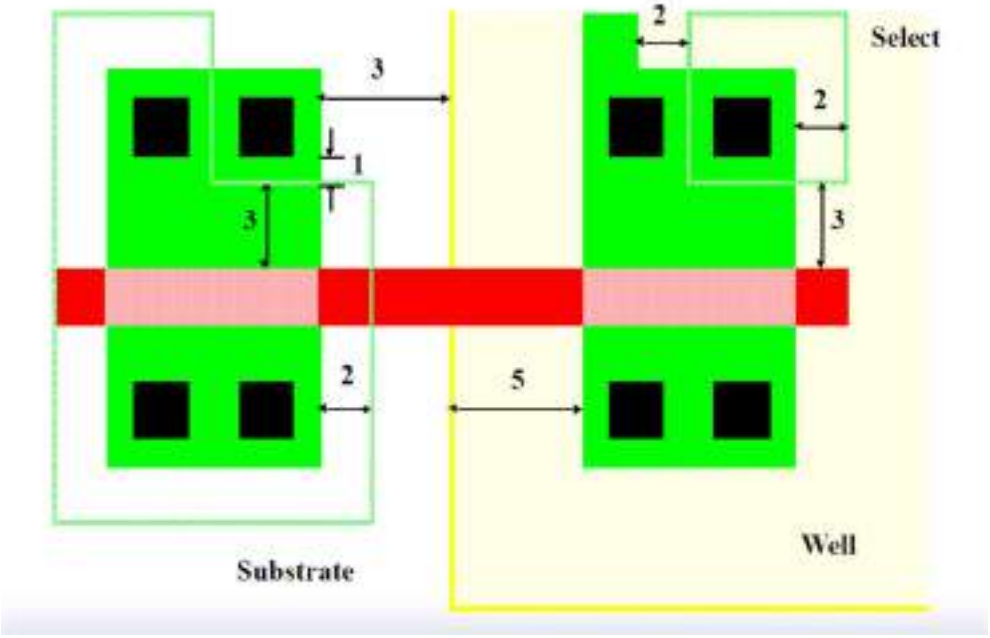
- Transistor layout



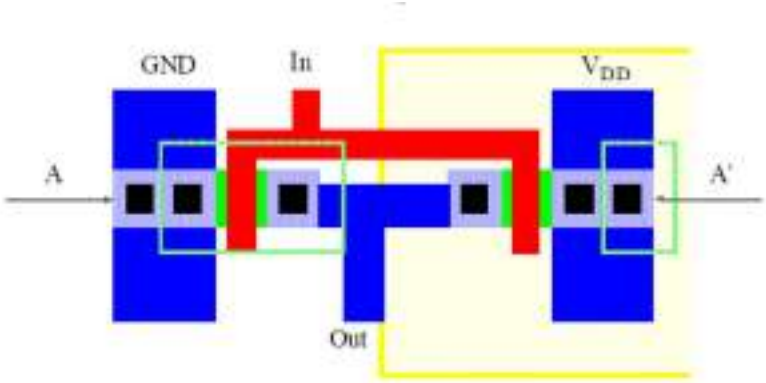
- Vias and Contacts



- Select layer



- CMOS inverter layout



Stick Diagram

- Stick diagram:
  - Shows all components and vias
  - Shows relative placement of components
  - Helps plan the lay out and routing
- Stick diagram does not show
  - Exact placement of components
  - Transistor size
  - Wite length, wire width, tub boundaries
  - Lo level details like parasitic
- Stick diagram – notations

- **Rule – 1**
  When two or more sticks of the same type cross or touch each other that represents electrical contact.

- **Rule – 2**

When two or more sticks of different type cross or touch each other there is no electrical contact. (If electrical contact is needed, we have to show the connection explicitly)

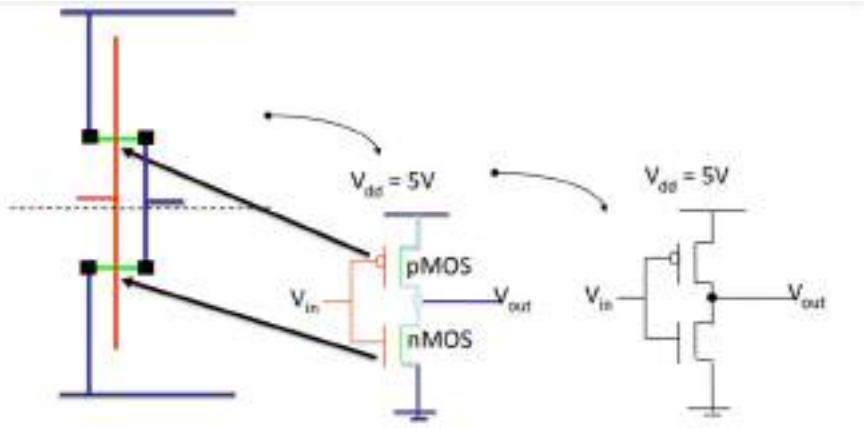
- **Rule – 3**
  When a poly crosses diffusion it represents a transistor

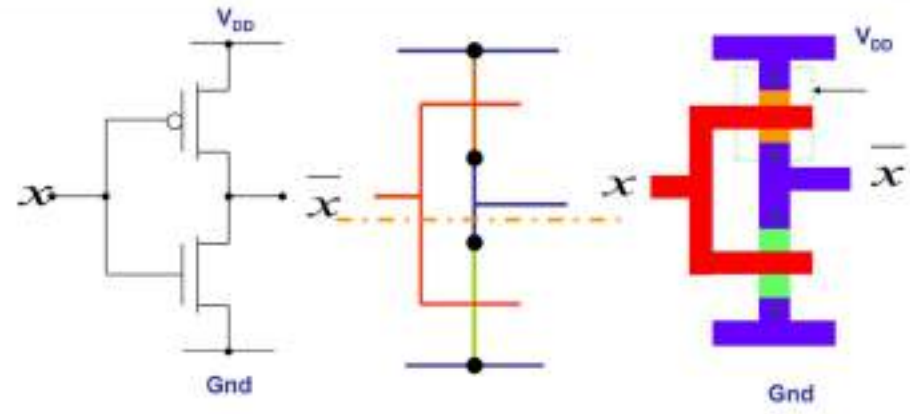
  When a poly crosses diffusion it represents a transistor

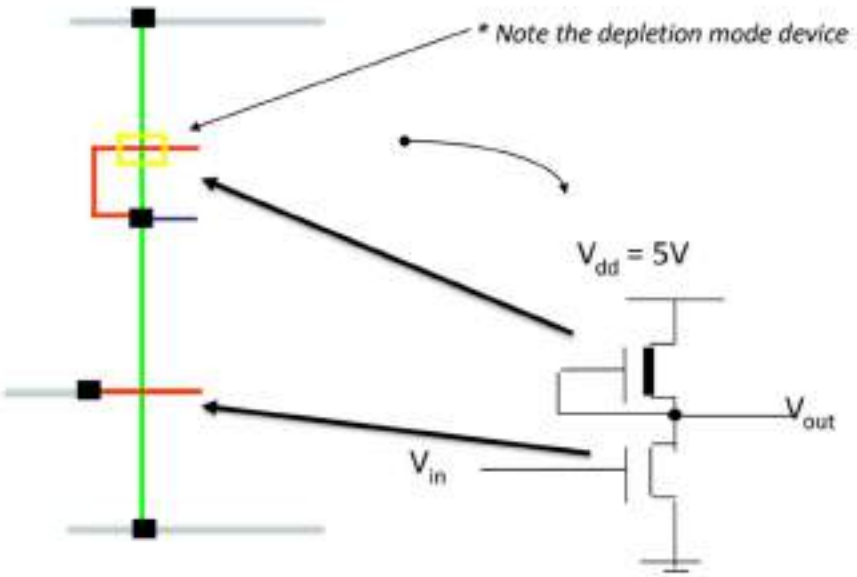
  Note: If a contact is shown then it is **not** a transistor

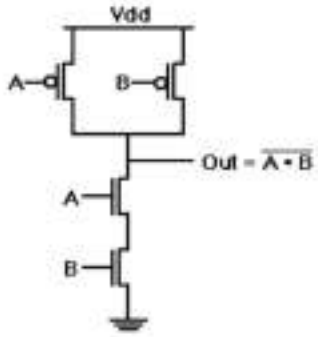
- **Rule – 4**
  In CMOS a demarcation line is drawn to avoid touching of p-diff with n-diff. All PMOS must lie on one side of the line and all NMOS will have to be on the other side.

- **Examples**


V_{dd} = 5V
pMOS
V_{in}
V_{out}
nMOS
V_{dd} = 5V
V_{in}
V_{out}


V_{DD}
x
$\overline{x}$
Gnd
V_{DD}
x
$\overline{x}$
Gnd


* Note the depletion mode device
V_{dd} = 5V
V_{out}
V_{in}



A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0