Discipline: 4TH SEM ELECTRONICS and Telecommunication Engineering			Name of the Teaching Faculty: Er. JYOTI PATRA & Er. KSHIRABDHEE TANAYA DORA	
Subject: - TH - 4No. of days per week classAnalog Electronics & Linear ICNo. of days per allotted: 3/5		eek class	Semester From Date: 14TH FEBRUARY 2023 to 23RD MAY 2023 No. of Weeks: 15	
Week	SN	Class Day	Theory Topics	
UNIT	-1: D	IODE, TR	RANSISTORS AND CIRCUITS. [10 PERIODS]	
1 st	1.	1 st	1.1 Working principle, of Diode & its current equation, Specification & use of p-n junction diode.	
1	2.	2 nd	1.2 Breakdown of diode (Avlance & Zener Breakdown) Construction, working, Characteristics	
2 nd	3.	1 st 2 nd	1.3 Classification of Rectifiers and working of different types of Rectifiers- Half-Wave Rectifier, Full-Wave Rectifier (CT & BRIDGE type)	
	4.	2 nd	1.4 Working principle of p-n-p and n-p-n transistor, different types of	
3 rd	5.	1 st	transistor connection (CB, CE and CC) & input and output characteristics of transistor in different connections.	
_	6.	2 nd	1.5 Define ALPHA, BETA and GAMMA of transistors in various modes. Establish the Mathematical relationship between them.	
4 th	7.	1 st	1.6 Basic concept of Biasing, Types of Biasing, h-parameter model of	
4	8.	2 nd	BJT, load line (AC &DC) and determine the Q-point.	
5 th	9.	1 st	1.7 Types of Coupling, working principle & use of R-C Coupled Amplifier	
	10.	2 nd	& Frequency Responses of R-C coupled Amplifier & draw the curve.	
U	NIT	- 2 : AUD	IO POWER AMPLIFIERS. [08 PERIODS]	
6 th	11.	1 st 2 nd	1.1 Classify Power Amplifier & Differentiate between Voltage and Power Amplifier.	
	12.			
8 th	13.	1 st 2 nd	1.2 Working principle of different types of Power Amplifier (Class-A,	
	14.	1 st	Class-AB, Class-B and Class-C & Class D amplifier).	
9 th	15.	2 nd		
	16. 17.	2 1 st	1.3 Construction and working principle and advantages of Push Pull	
10 th	17.	2 nd	_ (Class-B) Amplifiers	
UNI	Т-3	: FIELD	EFFECT TRANSISTOR (FET). [10 PERIODS]	
a a th	19.	1 st	3.1 FET & its classifications & Differentiate between JFET & BJT.	
11 th	20.	2 nd	3.2 Construction, working principle & characteristics of JEFT & Explain	
12 th	21.	1 st	JEFT as an amplifier, parameters of JFET & Establish relation among	
12"	22.	2 nd	JFET parameters.	
13 th	23.	1 st	3.3 Construction & working principle MOSFET & its classification &	
13	24.	2 nd	characteristics (Drain & Transfer)	
14 th	25.	1 st	- 3.4 Explain the operation of CMOS, VMOS & LDMOS.	
14	26.	2 nd		
15 th	27.	1 st	3.1 FET & its classifications & Differentiate between JFET & BJT.	
10	28.	2 nd		

Week	SN	Class Day	Theory Topics			
	Unit	-4: FEEDE	BACK AMPLIFIER & OSCILLATOR (8P)			
	1.	1 st	4.1 Define & classify Feedback Amplifier, principle of negative feedback with the help of block diagram, Types of feedback – negative & positive feedback.			
1 st	2.	2^{nd}	4.2 Types of negative feedback – voltage shunt, voltage series, (voltage gain, bandwidth , input Impedance output impedance) (contd)			
	3.	3 rd	4.2 Current shunt & Current series and characteristics voltage gain, bandwidth, input Impedance output (contd)			
	4.	1^{st}	4.2 Stability, noise, distortion in amplifiers			
2 nd	5.	2 nd	4.3 Oscillator -block diagram of sine wave oscillator ,Types Requirement of oscillation Barkhausen criterion			
	6.	3 rd	4.4 RC oscillators – RC phase shift: Circuit operation, circuit diagram, equation for frequency of oscillation (contd)			
	7.	1 st	4.4 Wien Bridge Oscillators: Circuit operation, circuit diagram, equation for frequency (contd)			
3 rd	8.	2 nd	4.4 Crystal, LC oscillators – Colpitts , Hartley :Circuit operation, circuit diagram, equation for frequency of oscillation & frequency stability			
5		UNIT-6:OPERATIONAL AMPLIFIER CIRCUITS & FEEDBACK CONFIGURATIONS (14P)				
	9.	3 rd	6.1 Differential amplifier & explain its configuration & significance.			
	10.	1 st	6.1 Differential amplifier & explain its configuration & significance.			
4 th	11.	2 nd	6.2 Block diagram representation of a typical Op- Amp, its equivalent circuits and draw the schematic symbol			
	12.	3 rd	6.4 Define the following electrical characteristics input offset voltage, input offset current (contd)			
	13.	1 st	6.4 Define CMMR, Large signal voltage gain, Slew rate			
5 th	14.	2 nd	6.5 Draw & explain Open Loop configuration (inverting, non-inverting Amplifier)			
	15.	3 rd	6.6 Draw the circuit diagram of the voltage series feedback amplifier and derive the close loop Voltage gain (contd)			
	16.	1 st	6.6 gain of feedback circuits input resistance, and output resistance (contd)			
6 th	17.	2 nd	6.6 bandwidth and total output offset voltage with feedback.			
	18.	3 rd	6.7 Draw the circuit diagram of the voltage shunt feedback amplifier and derive the close loop voltage gain			
	19.	1 st	6.7 Gain of feedback circuits input resistance, and output resistance (contd)			
7 th	20.	2 nd	6.7 bandwidth and total output offset voltage with feedback.			
	21.	3 rd	6.3 Discuss the types of integrated circuits manufacturer's designations of ICs, Package types, (contd)			
	22.	1^{st}	6.3 Discuss pin identification and temperature and ordering information.			
8 th	U		PPLICATION OF OPERATIONAL AMPLIFIER, TIMER RCUITS& IC VOLTAGE REGULATOR (13P)			

	23.	2^{nd}	7.1 Discuss the summing scaling and averaging of inverting amplifiers
	24.	3 rd	7.1 Discuss the summing scaling and averaging of non-inverting amplifiers
	25.	1 st	7.2 DC & AC Amplifies using OP-AMP.
9 th	26.	2 nd	7.3 Integrator using op-amp
	27.	3 rd	7.3 differentiator using op-amp
	28.	1 st	7.4 Active filter & describe the filter design of fast order low Pass Butterworth
10 th	29.	2 nd	7.5 Concept of Zero-Crossing Detector using Op-Amp
	30.	3 rd	7.6 Block diagram and operation of IC 555 timer &IC 565 PLL& its applications.
	31.	1^{st}	7.7 Working of Current to voltage Convertor using Operational Amplifier
11 th	32.	2 nd	7.8 Working of Voltage to Frequency Convertor using Operational Amplifier.
	33.	3 rd	7.9 Working of Frequency to Voltage Conversion using Operational Amplifier.
			7.10 Operation of neuron cumply using 70VV and 70VV IM 217 Series with their
	34.	1^{st}	
	34. 35.	1 st 2 nd	7.10 Operation of power supply using 78XX and 79XX,LM 317 Series with their PIN configuration7.11 Functional block diagram & Working of IC regulator LM 723 & LM 317
12 th	35.	2 nd	PIN configuration
12 th	35.	2 nd	PIN configuration 7.11 Functional block diagram & Working of IC regulator LM 723 & LM 317 UNED AMPLIFIER & WAVE SHAPING CIRCUIT (12P) 5.1 Defined and classify Tuned amplifier, Explain parallel Resonant circuit,
12 th	35. UN	2 nd	PIN configuration 7.11 Functional block diagram & Working of IC regulator LM 723 & LM 317 UNED AMPLIFIER & WAVE SHAPING CIRCUIT (12P)
12 th	35. UN 36.	2 nd NIT-5: T 3 rd	PIN configuration 7.11 Functional block diagram & Working of IC regulator LM 723 & LM 317 UNED AMPLIFIER & WAVE SHAPING CIRCUIT (12P) 5.1 Defined and classify Tuned amplifier, Explain parallel Resonant circuit, Resonance Curve & sharpness of Resonance.
	35. UN 36. 37.	2 nd NIT-5: T 3 rd 1 st	PIN configuration 7.11 Functional block diagram & Working of IC regulator LM 723 & LM 317 UNED AMPLIFIER & WAVE SHAPING CIRCUIT (12P) 5.1 Defined and classify Tuned amplifier, Explain parallel Resonant circuit, Resonance Curve & sharpness of Resonance. 5.2 Working principle of Single tuned Voltage Amplifier & its limitation (contd)
	35. UN 36. 37. 38.	2 nd NIT-5: T 3 rd 1 st 2 nd	PIN configuration 7.11 Functional block diagram & Working of IC regulator LM 723 & LM 317 UNED AMPLIFIER & WAVE SHAPING CIRCUIT (12P) 5.1 Defined and classify Tuned amplifier, Explain parallel Resonant circuit, Resonance Curve & sharpness of Resonance. 5.2 Working principle of Single tuned Voltage Amplifier & its limitation (contd) 5.2 Working principle of Double tuned Amplifier & its limitation
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13 th	35. UN 36. 37. 38. 39. 40.	2 nd IIT-5: T 3 rd 1 st 2 nd 3 rd 1 st 1 st	PIN configuration 7.11 Functional block diagram & Working of IC regulator LM 723 & LM 317 UNED AMPLIFIER & WAVE SHAPING CIRCUIT (12P) 5.1 Defined and classify Tuned amplifier, Explain parallel Resonant circuit, Resonance Curve & sharpness of Resonance. 5.2 Working principle of Single tuned Voltage Amplifier & its limitation (contd) 5.2 Working principle of Double tuned Amplifier & its limitation 5.3 Different type of Non-linear circuits - Clipper, diode series & shunt (contd) 5.3 Positive& negative biased & unbiased clipper (contd) 5.3 Combinational clipper clippers circuit & its application 5.4 Different type of Clamper circuit (positive & negative clampers) & its
13 th	35. UN 36. 37. 38. 39. 40. 41.	2^{nd} JIT-5: T 3^{rd} 1^{st} 2^{nd} 3^{rd} 1^{st} 2^{nd}	PIN configuration 7.11 Functional block diagram & Working of IC regulator LM 723 & LM 317 UNED AMPLIFIER & WAVE SHAPING CIRCUIT (12P) 5.1 Defined and classify Tuned amplifier, Explain parallel Resonant circuit, Resonance Curve & sharpness of Resonance. 5.2 Working principle of Single tuned Voltage Amplifier & its limitation (contd) 5.2 Working principle of Double tuned Amplifier & its limitation 5.3 Different type of Non-linear circuits - Clipper, diode series & shunt (contd) 5.3 Positive& negative biased & unbiased clipper (contd) 5.3 Combinational clipper clippers circuit & its application
13 th	35. UN 36. 37. 38. 39. 40. 41. 42.	2 nd IIT-5: T 3 rd 1 st 2 nd 3 rd 1 st 2 nd 3 rd 1 st 2 nd 3 rd	PIN configuration 7.11 Functional block diagram & Working of IC regulator LM 723 & LM 317 UNED AMPLIFIER & WAVE SHAPING CIRCUIT (12P) 5.1 Defined and classify Tuned amplifier, Explain parallel Resonant circuit, Resonance Curve & sharpness of Resonance. 5.2 Working principle of Single tuned Voltage Amplifier & its limitation (contd) 5.2 Working principle of Double tuned Amplifier & its limitation 5.3 Different type of Non-linear circuits - Clipper, diode series & shunt (contd) 5.3 Positive& negative biased & unbiased clipper (contd) 5.3 Combinational clipper clippers circuit & its application 5.4 Different type of Clamper circuit (positive & negative clampers) & its
13 th 14 th	35. UN 36. 37. 38. 39. 40. 41. 42. 43.	2^{nd} AIT-5: T 3^{rd} 1^{st} 2^{nd} 3^{rd} 1^{st} 2^{nd} 3^{rd} 1^{st} 2^{nd} 1^{st} 2^{nd} 1^{st} 1^{st} 2^{nd} 1^{st} 2^{nd} 1^{st} 1^{st} 2^{nd} 1^{st} 2^{nd} 1^{st} 1^{st} 2^{nd} 1^{st} 1^{st} 2^{nd} 1^{st} 2^{nd} 1^{st} 2^{nd} 1^{st} 2^{nd} 1^{st} 2^{nd} 1^{st} 2^{nd} 1^{st} 2^{nd} 1^{st} 3^{rd} 1^{st} 3^{rd} 3^{rd} 3^{rd} 3^{rd} 1^{st}	PIN configuration 7.11 Functional block diagram & Working of IC regulator LM 723 & LM 317 UNED AMPLIFIER & WAVE SHAPING CIRCUIT (12P) 5.1 Defined and classify Tuned amplifier, Explain parallel Resonant circuit, Resonance Curve & sharpness of Resonance. 5.2 Working principle of Single tuned Voltage Amplifier & its limitation (contd) 5.2 Working principle of Double tuned Amplifier & its limitation 5.3 Different type of Non-linear circuits - Clipper, diode series & shunt (contd) 5.3 Positive& negative biased & unbiased clipper (contd) 5.3 Combinational clipper clippers circuit & its application 5.4 Different type of Clamper circuit (positive & negative clampers) & its application. 5.5 Working principle of Astable, Monostable and Bistable Multivibrator with
13 th 14 th	35. UN 36. 37. 38. 39. 40. 41. 42. 43. 44.	2 nd JIT-5: T 3 rd 1 st 2 nd 3 rd 1 st 2 nd 3 rd 1 st 2 nd 3 rd	PIN configuration 7.11 Functional block diagram & Working of IC regulator LM 723 & LM 317 UNED AMPLIFIER & WAVE SHAPING CIRCUIT (12P) 5.1 Defined and classify Tuned amplifier, Explain parallel Resonant circuit, Resonance Curve & sharpness of Resonance. 5.2 Working principle of Single tuned Voltage Amplifier & its limitation (contd) 5.2 Working principle of Double tuned Amplifier & its limitation 5.3 Different type of Non-linear circuits - Clipper, diode series & shunt (contd) 5.3 Positive& negative biased & unbiased clipper (contd) 5.3 Combinational clipper clippers circuit & its application 5.4 Different type of Clamper circuit (positive & negative clampers) & its application. 5.5 Working principle of Astable, Monostable and Bistable Multivibrator with

TH2-DCCN-SEM4

S.No	Торіс	Contents To be covered:	Recourse	Class No in the week	Week
		Unit-1: Network& Protoco	l (8P)		
1	1.1 Data Communication	 Introduction Components of Communication Data Representation Network Criteria: 	1.Lecture Note 2.CCNA Module 1 1.Lecture Note	1	
2	1.2 Networks	 Performance Reliability Security 	2.CCNA Module 1	2	
3	1.2 Networks	Types of Networks: LAN MAN WAN PAN	1.Lecture Note 2.CCNA Module 1	3	1 st
4	1.3 OSI layer model(Applicati on, Presentation Session layer)	 Define: Protocol Standards Explain the necessity of Layered Tasks at sender and receiver Inro to OSI model Application and Session layer working 	1.Lecture Note 2.CCNA Module 1 3. Animation: https://www.y outube.com/w atch?v=- 6Uoku-M6oY	4	
5	1.3 OSI layer model(Transport , Network layer)	Functionality of:Transport layerNetwork layer	1.Lecture Note 2.CCNA Module 1	1	
6	1.3 OSI layer model(Datalink, Physical layer)	Functionality of: • Datalink layer • Physical layer	1.Lecture Note 2.CCNA Module 1	2	2 ND
7	1.3 TCP/IP	 Intro to TCP/IP Comparison between TCP/IP and OSI architecture 	1.Lecture Note 2.CCNA Module 1	3	
8	1.3 Protocol & Architecture, Standards	 Protocol & Architecture, Standards Recap of 1st chapter 	1.Lecture Note 2.CCNA Module 1	4	
		Unit-7: TCP/IP (8P)			
9	7.1 TCP/IP Protocol Suite	In detail explanation of different layers of TCP/IP architecture	1.Lecture Note	1	
10	7.2 Basic Protocol functions	Explain the protocols of Application layer: HTTP,HTTPS,DNS,Telnet,SSH,FTP etc	1.Lecture Note	2	

11	7.2 Basic Protocol functions	Explain the protocols of Transport layer: • TCP • UDP • TCP vs UDP Explain the protocols of Internet layer: • IPv4: Classify and explain	1.Lecture Note 2.animation: https://www.y outube.com/w atch?v=A3zId8j OfV4 3. CCNA Module 1 1.Lecture Note 2. Nptel:	3	3 RD
12	7.4 Internet Protocol operations	different classes of IPv4	https://www.y outube.com/w atch?v=5vbPS- Knhvl 3. CCNA Module 1		
13	7.4 Internet Protocol operations	Classes addressingSubnet Mask	1.Lecture Note 3. CCNA Module 1	1	
14	7.3 Internet Protocol operations	IPv4 header	1.Lecture Note	2	
15	7.4 Internet Protocol	 Explain the protocols of Internet layer: IPv6 representation Ipv6 header and applications IPv4 vs Ipv6 	1.Lecture Note 2. CCNA Module 1	3	4 ^{тн}
16	7.3 Principles of Internetworking	 Extranet Intranet Internet Revision of entire chapter 	1.Lecture Note 2. video link: <u>https://www.y</u> <u>outube.com/w</u> <u>atch?v=YMP5-</u> <u>Zynuw4</u> 2. CCNA Module 1	4	
	UNIT	- 2. DATA TRANSMISSION &	MEDIA (8P)		
17	2.1 Data transmission Concepts and Terminology	 Modes of transmission: Simplex, Half Duplex, Full Duplex Types of Connection: Point-to- Point, Multipoint 	1.Lecture Note 2. animation: https://www.y outube.com/w atch?v=LMRSS 7ZYM50	1	
18	2.1 Data transmission Concepts and Terminology	 Brief explanation on: Channel (Analog/digital) Data transfer rate Throughput Bandwidth 	1.Lecture Note	2	5 [™]

19	2.2 Analog and Digital Data transmission	Analog SignalDigital SignalAnalog Transmission	1.Lecture Note	3	
20	2.2 Analog and Digital Data transmission	 Digital Transmission Comparison between Analog and Digital Transmission 	1.Lecture Note 2. Video: <u>https://www.y</u> <u>outube.com/w</u> <u>atch?v=33kbeb</u> <u>X5fkk</u>	4	
21	2.3 Transmission impairments, Channel capacity	 Explain: Attenuation, Distortion, Types of noise (Thermal noise, intermodal noise, impulse noise) crosstalk 	1.Lecture Note 2.video: <u>https://www.y</u> <u>outube.com/w</u> <u>atch?v=Ey75NV</u> <u>Q6qYE</u> 3. Video: <u>https://www.y</u> <u>outube.com/w</u> <u>atch?v=FCk_pD</u> <u>Cc-x4</u>	1	6 ^{тн}
22	2.3 Transmission impairments, Channel capacity	Channel CapacityShannon channel capacity formula	1.Lecture Note	2	
23	2.4 Transmission media, Guided Transmission, Wireless Transmission	 Classify media Explain the guided media (twisted pair and coaxial cable) 	1.Lecture Note 2.video: <u>https://www.y</u> <u>outube.com/w</u> <u>atch?v=fgOkvIH</u> <u>KgXQ</u> 3.CCNA MODULE 1	3	
24	2.4 Transmission media, Guided Transmission, Wireless Transmission	 Explain the guided media- optical fiber cable Explain the unguided media 	1.Lecture Note 2.CCNA Module 1	4	-
		Unit-3. Data Encoding (8	SP)	1	<u>.</u>
25	3.1 Data encoding,	Define: • Encoding, • Data Encoding Types of Data Encoding	1.Lecture Note	1	
26	3.2 Digital data digital signals	 Different techniques used for Digital data digital signal encoding Unipolar encoding Polar: NRZ encoding 	1.Lecture Note	2	7 TH

27	3.2 Digital data digital signals	RZ encodingManchester encodingBiphase encoding	1.Lecture Note	3	
28	3.3 Digital data analog signals	Digital Analog conversionASK	1.Lecture Note 2. video: https://www.y outube.com/w atch?v=mHvV Tv8HDQ	4	
29	3.3 Digital data analog signals	FSKPSK	1.Lecture Note 2. video: https://www.y outube.com/w atch?v=mHvV Tv8HDQ	1	8 TH
30	3.4 Analog data digital signals	Pulse code modulation and its block diagram	1.Lecture Note 2. video: https://www.y outube.com/w atch?v=mHvV Tv8HDQ	2	
31	3.5 Analog data analog signals	 Analog data anlog signal AM 	1.Lecture Note 2. video: https://www.y outube.com/w atch?v=mHvV Tv8HDQ	3	
32	3.5 Analog data analog signals	FMPM	1.Lecture Note 2. video: https://www.y outube.com/w atch?v=mHvV Tv8HDQ	4	
	Unit-4. Da	ata Communication & Data	link control ((8P)	
33	4.1 Asynchronous and Synchronous Transmission	 Asynchronous Transmission Synchronous Transmission 	1.Lecture Note	1	
34	4.2 Error Detection	Parit checkChecksumCyclic redundancy check	1.Lecture Note	2	9 [™]
35	4.3 Line configuration	 Point to point configuration Multipoint configuration 	1.Lecture Note	3	
36	4.4 Flow Control	 Stop and wait protocol 	1.Lecture Note	4	

		Sliding widnow protocol			
37	4.5 Error Control	 Single bit error vs burst error Stop and wait arq Go back n Selective reject 	1.Lecture Note Video: <u>https://www.y</u> <u>outube.com/w</u> <u>atch?v=kSgtZnf</u> <u>fCog</u>	1	10 TH
38	4.6 Multiplexing	 Reasons for multiplexing Typs of multiplexing Advantages 		2	
39	4.7 FDM synchronous TDM	 FDM TDM(Synchronous) 	1.Lecture Note 2.video: https://www.y outube.com/w atch?v=f52bwN buMDA 3.video: https://www.y outube.com/w atch?v=aeJ55Iy SP_I	3	
40	4.8 Statistical TDM	Statistical TDM	1.Lecture Note	4	
		Unit-6: LAN Technology (10P)		
41	6.1. Topology	 Define topology Explain different types of topology(Contd) 	1.Lecture Note 2. CCNA Module 1 3. video: <u>https://www.y</u> <u>outube.com/w</u> <u>atch?v=zbqrNg</u> <u>4C98U</u>	1	11 TH
42	6.1 Topology	Explain different types of topology	1.Lecture Note	2	
43	6.2 LAN protocol architecture	Features of LANLogic link layer	1.Lecture Note	3	
44	6.3. Medium Access control	 Channel allocation and types Pure Aloha Slotted Aloha 	1.Lecture Note 2. video: <u>https://www.y</u> <u>outube.com/w</u> <u>atch?v=j4-</u> <u>r0e7DjqY</u>	4	
45	6.3. Medium Access control	CSMA/CDCSMA/CA	1.Lecture Note 2. Video: <u>https://www.y</u> <u>outube.com/w</u>	1	

			atch?v=KDHbP 81SAmA		12 [™]
46	6.4 Bridges, Hub, Switch	RepeaterHub	1.Lecture Note 2. animation: https://www.y outube.com/w atch?v=1z0ULv g_pW8	2	
47	6.4 Bridges, Hub, Switch	SwitchRouterGateway	1.Lecture Note 2. animation: https://www.y outube.com/w atch?v=1z0ULv g_pW8	3	
48	6.5 Ethernet (CSMA/CD)	Explain the concept of Ethernet	1.Lecture Note 2. video: https://www.y outube.com/w atch?v=i2qiNA VfQRw	4	
49	6.5 Fiber Channel	Explain the fiber channel	1.Lecture Note	1	13 [™]
50	6.6 Wireless LAN Technology	Wireless LAN Technology	1.Lecture Note 2.video: https://www.y outube.com/w atch?v=METB1 o4UAT8	2	10
		Unit-5: Switching & Routing	(10P)	1	
51	5.1 Circuit Switching networks	 Concept of Routing and switching Circuit switching Advantages and disadvantages 	1.Lecture Note 2. Video: https://www.y outube.com/w atch?v=- HJJ4psu5aU&t= 77s	3	13 TH
52	5.2 Packet Switching principles	 Packet switching Advantages and disadvantages Differences between circuit and packet switching 	1.Lecture Note 2. <u>https://www.y</u> <u>outube.com/w</u> <u>atch?v=-</u> <u>HIJ4psu5aU&t=</u> <u>77s</u>	4	

53	5.3 X.25	X.25	1.Lecture Note 2. nptel: https://www.y outube.com/w atch?v=DU7IZ MciHJE	1	TH
54	5.4 Routing in Packet switching	 Centralized vs Distributed Routing Static vs Dynamic Routing Virtual Circuit Based Packet Switching Datagram Circuit Based Packet Switching 	1.Lecture Note	2	14 TH
55	5.5 Congestion	 Causes of Congestion Congestion correction 	1.Lecture Note 2.video: https://www.y outube.com/w atch?v=txctUW Firt8	3	
56	5.6 Effects of congestion, congestion control	Congestion Control:Open loop Congestion control	1.Lecture Note 2. https://www.y outube.com/w atch?v=txctUW Firt8	4	
57	5.6 Effects of congestion, congestion control	Congestion Control:Close loop Congestion control	1.Lecture Note 2. video: https://www.y outube.com/w atch?v=ZYId YIt7W_g	1	15 [™]
58	5.7 Traffic Management	 Types of network traffic Traffic management techniques 	1.Lecture Note	2	
59	5.8 Congestion Control in Packet Switching Network.	Congestion Control in Packet Switching Network.	1.Lecture Note	3	
60	5.8 Congestion Control in Packet Switching Network.	Revision of chapter 5	1.Lecture Note	4	

Discipline: 4TH SEM ELECTRONICS and Telecommunication Engineering			Name of the Teaching Faculty: Er. GOPAL CH. BEHERA & Er. POONAM PANDA
Subject: - TH - 3No. of days perMicroprocessor &week classMicrocontrollerallotted: 05		eek class	Semester From Date: 14 TH FEBRUARY 2023 to 23 RD MAY 2023 No. of Weeks: 15
Week	SN	Class Day	Syllabus To be Covered [SESSION: 2022-23]
UNIT-1: MIC		PROCES	SOR (Architecture & Programming-8085-8-bit) [] 15P
	1.	1 st	1.1 Introduction to Microprocessor and Microcomputer & distinguish between them.
	2.	2 nd	1.2 Concept of Address bus, Data bus, Control Bus & System Bus
1 st	3.	3 rd	1.3 General Bus structure Block Diagram.
	4.	4 th	1.3 General Bus structure Block Diagram.
	5.	5 th	1.4 Basic Architecture of 8085 (8 bit) Microprocessor
	6.	1 st	1.4 Basic Architecture of 8085 (8 bit) Microprocessor
	7.	2 nd	1.4 Basic Architecture of 8085 (8 bit) Microprocessor
2 nd	8.	3 rd	1.5 Signal Description (Pin Diagram) of 8085 Microprocessor
—	9.	4 th	1.5 Signal Description (Pin Diagram) of 8085 Microprocessor
	10.	5 th	1.5 Signal Description (Pin Diagram) of 8085 Microprocessor
	11.	1 st	1.6 Register Organizations, Distinguish between SPR & GPR
	12.	2 nd	1.6 Timing & Control Module,
3 rd	13.	- 3 rd	1.7 Stack, Stack pointer & Stack top.
U	14.	4 th	1.7 Stack, Stack pointer & Stack top.
	15.	5 th	1.8 Interrupts:-8085 Interrupts, Masking of Interrupt (SIM, RIM)
		-	truction Set & Assembly Language Programming [] 15P
			2.1 Addressing data & Differentiate between one-byte, two-byte &
	16.	1 st	three-byte instructions with examples.
4 th	17.	2 nd	2.2 Addressing modes in instructions with suitable examples.
	18.	3 rd	2.3 Instruction Set of 8085 (Data Transfer)
	19.	4 th	2.3 Instruction Set of 8085 (Arithmetic, Logical)
	20.	5 th	2.3 Instruction Set of 8085 (Branching)
	21.	1 st	2.3 Instruction Set of 8085 (Stack & I/O, Machine Control)
	22.	2 nd	2.4 Simple ALP of 8085; 2.4.1 Simple Addition & Subtraction
5 th	23.	3 rd	2.4.2 Logic Operations (AND, OR, Complement 1's & 2's) & Masking of bits
5	24.	4 th	2.4.3 Counters & Time delay (Single Register, Register Pair, More than Two Register)
	25.	5 th	2.4.4 Looping, Counting & Indexing (Call/JMP etc).
	26.	1 st	2.4.5 Stack & Subroutine Programs.
	27.	2 nd	2.4.6 Code conversion, BCD Arithmetic & 16 Bit data Operation, Block Transfer
6 th	28.	3 rd	2.4.7 Compare between two numbers
U	29.	4 th	2.4.8 Array Handling (Largest number & smallest number in the array
	30.	5 th	2.5 Memory & I/O Addressing
		UNIT	
	31.	1 st	3.1 Define Opcode, operand, T-State, Fetch cycle, Machine Cycle,
# th	32.	2 nd	3.1 Instruction cycle & discuss the concept of timing diagram.
7 th	33.	3 rd	3.2 Draw timing diagram for memory read, memory write machine cycle.
	34.	4 th	3.2 Draw timing diagram for I/O read, I/O write machine cycle.
	35.	5 th	3.3 Draw a neat sketch for timing diagram for 8085 (MOV Instruction

	36.	1 st	3.3 Draw a neat sketch for timing diagram for 8085 (MOV Instruction).			
	37.	2 nd	3.3 Draw a neat sketch for timing diagram for 8085 (MVI Instruction).			
	38.	3 rd	3.3 Draw a neat sketch for timing diagram for 8085 (LDA Instruction).			
8 th		[T-4	Microprocessor Based System Development AIDS []10P			
	39.	4 th	4.1 Concept of interfacing			
	40.	5 th	4.2 Define Mapping & Data transfer mechanisms - Memory mapping & I/O Mapping			
		-	4.3 Concept of Memory Interfacing:- Interfacing EPROM & RAM			
	41.	1 st	Memories. 4.4 Concept of Address decoding for I/O devices			
Oth	42.	2 nd	4.5 Programmable Peripheral Interface: 8255			
9 th	43.	3 rd	4.6 ADC & DAC with Interfacing.			
	44.	4 th	4.7 Interfacing Seven Segment Displays			
	45.	5 th	4.8 Generate square waves on all lines of 8255			
	46.	1^{st}	4.9 Design Interface a traffic light control system using 8255.			
	47.	2 nd	4.10 Design interface for stepper motor control using 8255.			
1 Ath	48.	3 rd	4.11 Basic concept of other Interfacing DMA controller, USART			
10 th	UNI	T-5 Mic	roprocessor (Architecture & Programming-8086-16 bit) 🛛 12P			
	49.	4 th	5.1 Register Organization of 8086			
	50.	5 th	5.2 Internal architecture of 8086			
	51.	1 st	5.2 Internal architecture of 8086			
	52.	2 nd	5.3 Signal Description of 8086			
11 th	53.	3 rd	5.3 Signal Description of 8086			
	54.	4 th	5.4 General Bus Operation & Physical Memory Organization			
	55.	5 th	5.5 Minimum Mode & Timings, 5.6 Maximum Mode & Timings,			
	56.	1^{st}	5.7 Interrupts and Interrupt Service Routines, Interrupt Cycle, Non-Maskable Interrupt, Maskable Interrupt			
1 Oth	57.	2^{nd}	5.8 8086 Instruction Set & Programming: Addressing Modes, Instruction Set			
12 th	58.	3 rd	5.8 8086 Instruction Set & Programming: Assembler Directives and Operators			
	59.	4 th	5.9 Simple Assembly language programming using 8086 instructions.			
	60.	5 th	5.9 Simple Assembly language programming using 8086 instructions.			
	U	UNIT-6 Microcontroller (Architecture and Programming-8 bit)[15				
	61.	1^{st}	6.1 Distinguish between Microprocessor & Microcontroller			
13 th	62.	2 nd	6.2 8 bit & 16 bit microcontroller. 6.3 CISC & RISC processor			
	63.	3 rd	6.4 Architecture of 8051 Microcontroller			
	64.	4 th	6.4 Architecture of 8051 Microcontroller			
	65.	5 th	6.5 Signal Description of 8051 Microcontrollers			
	66.	1^{st}	6.6 Memory Organization-RAM structure, SFR			
14 th	67.	2^{nd}	6.7 Registers, timers, interrupts of 8051 Microcontrollers			
14	68.	3 rd	6.7 Registers, timers, interrupts of 8051 Microcontrollers			
	69.	4 th	6.8 Addressing Modes of 8051			
	70.	5 th	6.9 Simple 8051 ALP: - Arithmetic & Logic Instructions Programming			
	71.	1^{st}	6.9 Simple 8051 ALP: - JUMP, LOOP Instructions Programming			
	72.	2 nd	6.9 Simple 8051 ALP: - I/O Port Programming			
15 th	73.	3 rd	6.10 Interrupts, Timer & Counters			
	74.	4 th	6.11 Serial Communication			
	75.	5 th	6.12 Microcontroller Interrupts and Interfacing to 8255			